

# A Tree-based Modular SMT Solver

Georg Schadler  
Georg Hofferek

# Outline

- Motivation
- Proof structure, requirements & properties
- Implementation & example
- Theory checks & interpolation
- Outlook & conclusion

# Motivation

# Motivation

- Synthesize **multiple Boolean control signals** e.g. for a pipelined processor.
- Specification given as a **quantified first-order formula**.
- **Uninterpreted functions** to abstract specification

# Quantified Formula

 $\Psi =$  $\forall$  *inputs, states* .

Stuff that choice  
of control signals  
depends on

 $\exists$  *controlsignals* .

Correctness  
axiom

 $\forall$  *auxvars* . $\Phi$ 

Unknown  $\rightarrow$  To  
be synthesized

Stuff that control  
signals *do not*  
*depend on*

# Formula Expansion

$$\forall \vec{a} \exists c_0, c_1 \forall \vec{b} . \Phi(\vec{a}, \vec{b}, c_0, c_1) = \top$$

- Expansion of  $\exists$
- Renaming of  $\vec{b}$
- Negation

$$\neg \Phi(\vec{a}, \vec{b}_{00}, 0, 0) \wedge \neg \Phi(\vec{a}, \vec{b}_{10}, 1, 0) \wedge \neg \Phi(\vec{a}, \vec{b}_{01}, 0, 1) \wedge \neg \Phi(\vec{a}, \vec{b}_{11}, 1, 1) = \perp$$

“Partitions”:  $\phi_{00}, \phi_{01}, \phi_{10}, \phi_{11}$

# Motivation Recap

1. Construct unsatisfiable SMT formula from specification and compute proof
2. Craig interpolation to compute multiple coordinated interpolants.
3. Interpolants implement the Boolean control signals.

**More Information:**  
Hofferek et al., FMCAD 2013  
Hofferek & Bloem, MEMOCODE 2011

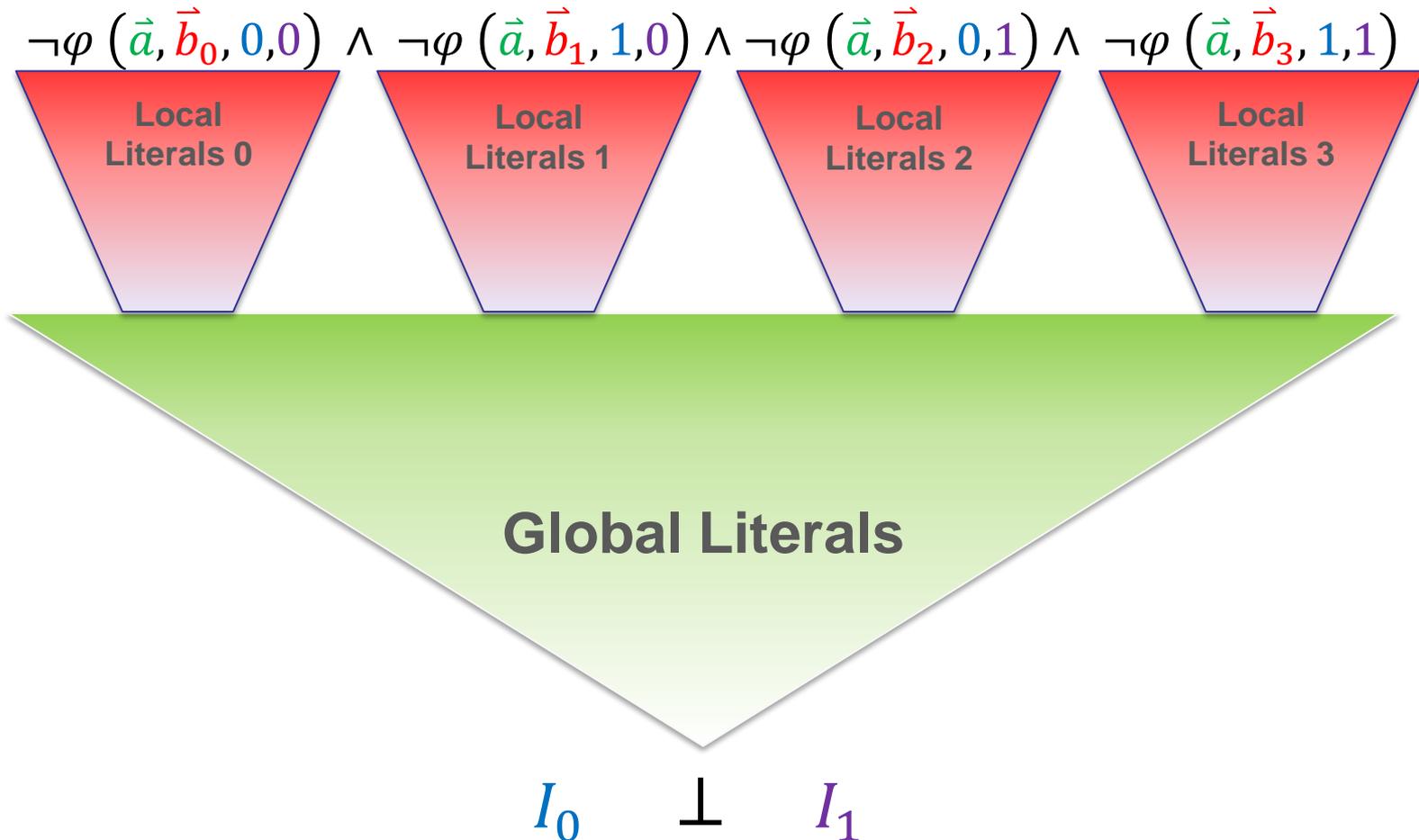
# Refutation Proof

- Proof requires two properties:
  - **Local-first**

Local literals are resolved before global literals
  - **Colorable**

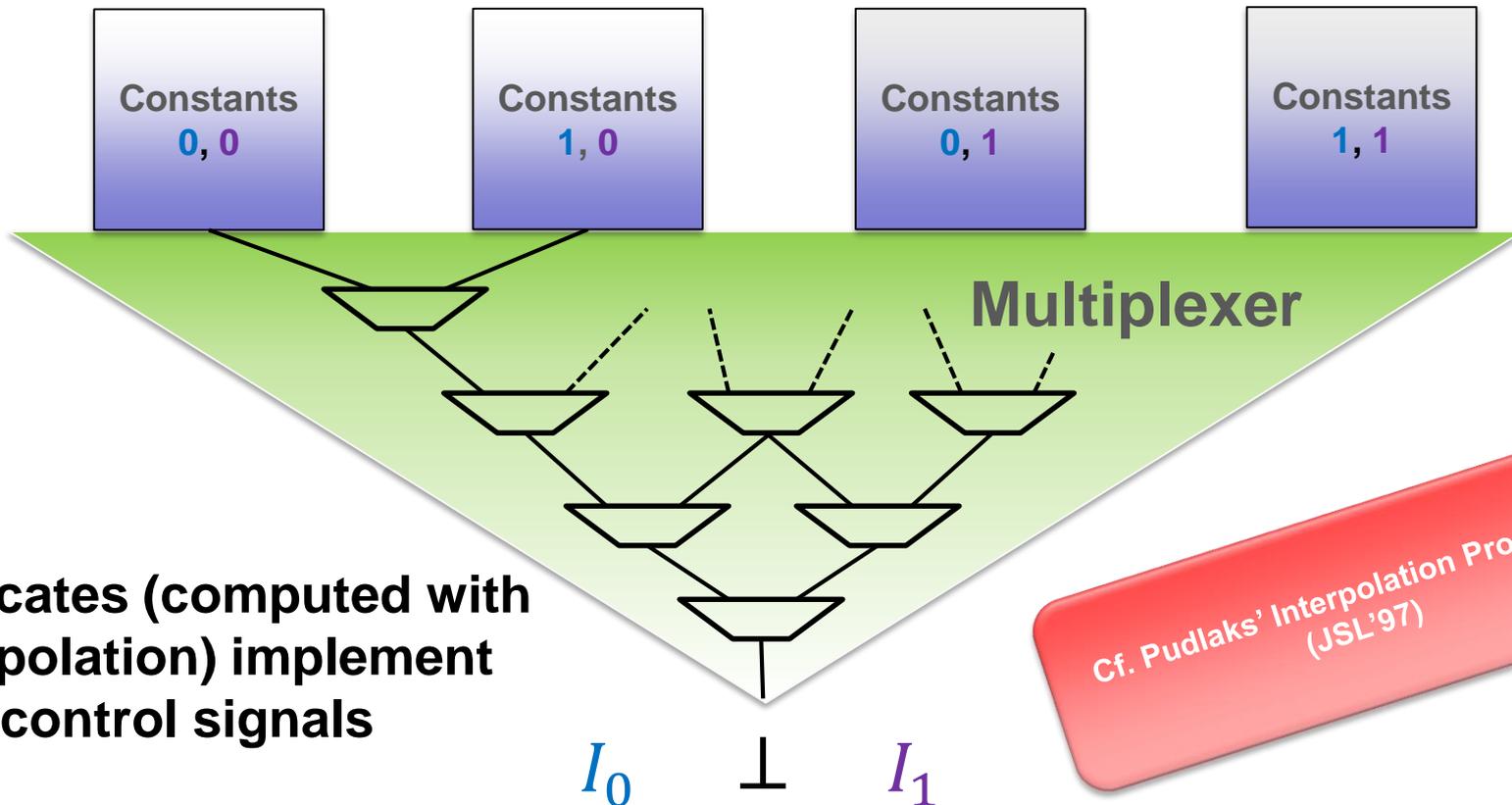
No literals or leaves with symbols from two partitions

# Proof Requirements



# Proof Requirements

$$\neg\varphi(\vec{a}, \vec{b}_0, 0, 0) \wedge \neg\varphi(\vec{a}, \vec{b}_1, 1, 0) \wedge \neg\varphi(\vec{a}, \vec{b}_2, 0, 1) \wedge \neg\varphi(\vec{a}, \vec{b}_3, 1, 1)$$



Cf. Pudlaks' Interpolation Procedure  
(JSL'97)

Certificates (computed with  
interpolation) implement  
control signals

# Colorability

Partitions  $\approx$  Colors:

$$\neg\Phi_{00}(\vec{a}, \vec{b}_{00}) \wedge \neg\Phi_{10}(\vec{a}, \vec{b}_{10}) \wedge \neg\Phi_{01}(\vec{a}, \vec{b}_{01}) \wedge \neg\Phi_{11}(\vec{a}, \vec{b}_{11})$$

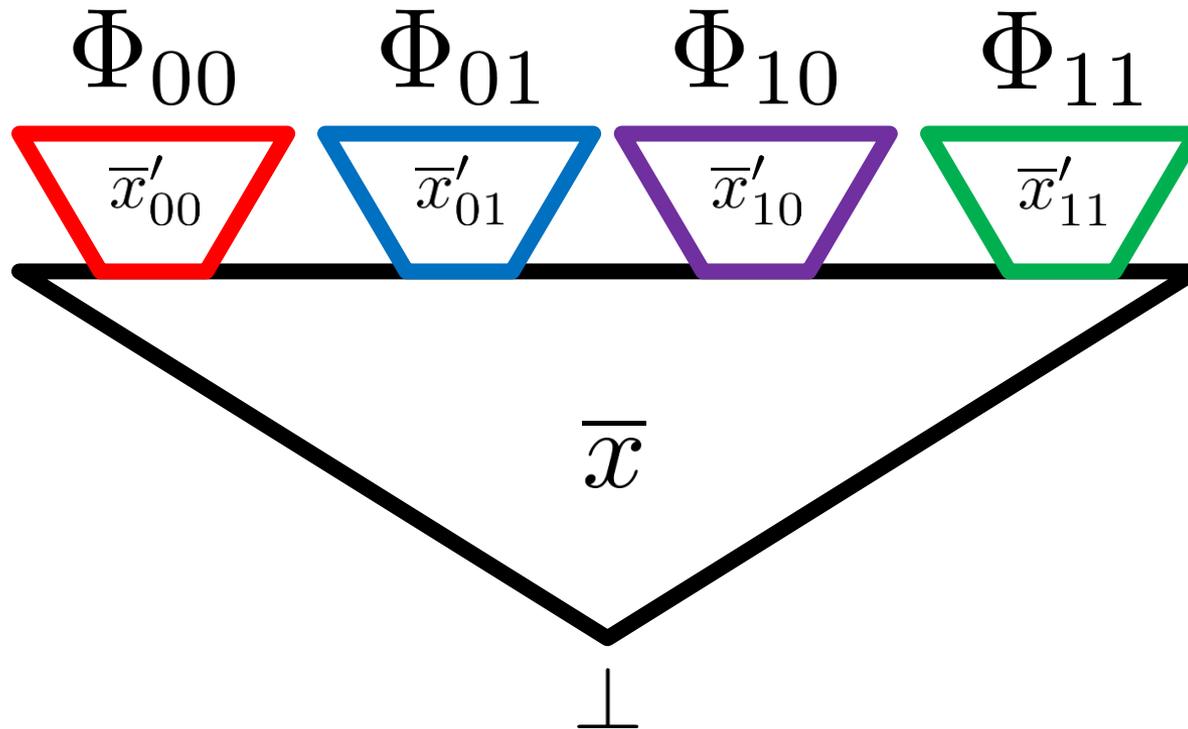
Local Symbols:  $\vec{b}_{00}$ ,  $\vec{b}_{10}$ ,  $\vec{b}_{01}$ ,  $\vec{b}_{11}$  (colored)

Global Symbols:  $\vec{a}$  (colorless)

Colorable:  $(x = y)$ ,  $(u = v)$ ,  $(w = z)$

Non-colorable:  $(x = u)$

# Colorability



**No literals or leaves with symbols from two partitions**

# Implementation

# Implementation

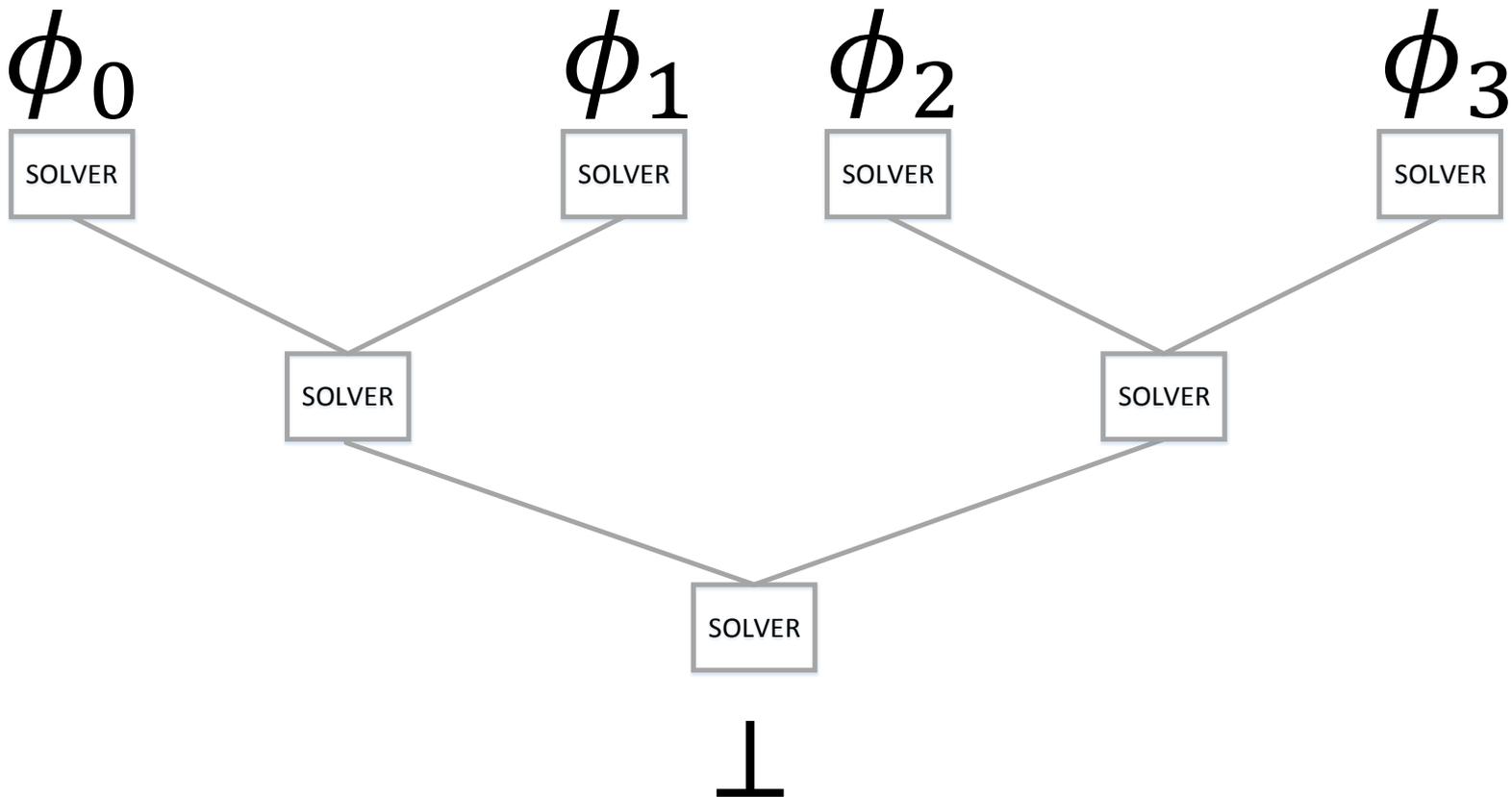
Control signals can depend on inputs that are independent from each other

$$\forall \vec{a} \exists \vec{c} \forall \vec{a}' \exists \vec{c}' \forall \vec{a}'' \exists \vec{c}'' \dots . \Phi$$

- 1 level per  $\forall \exists$  - alternation
- $2^{|\vec{a}|}$  nodes per level

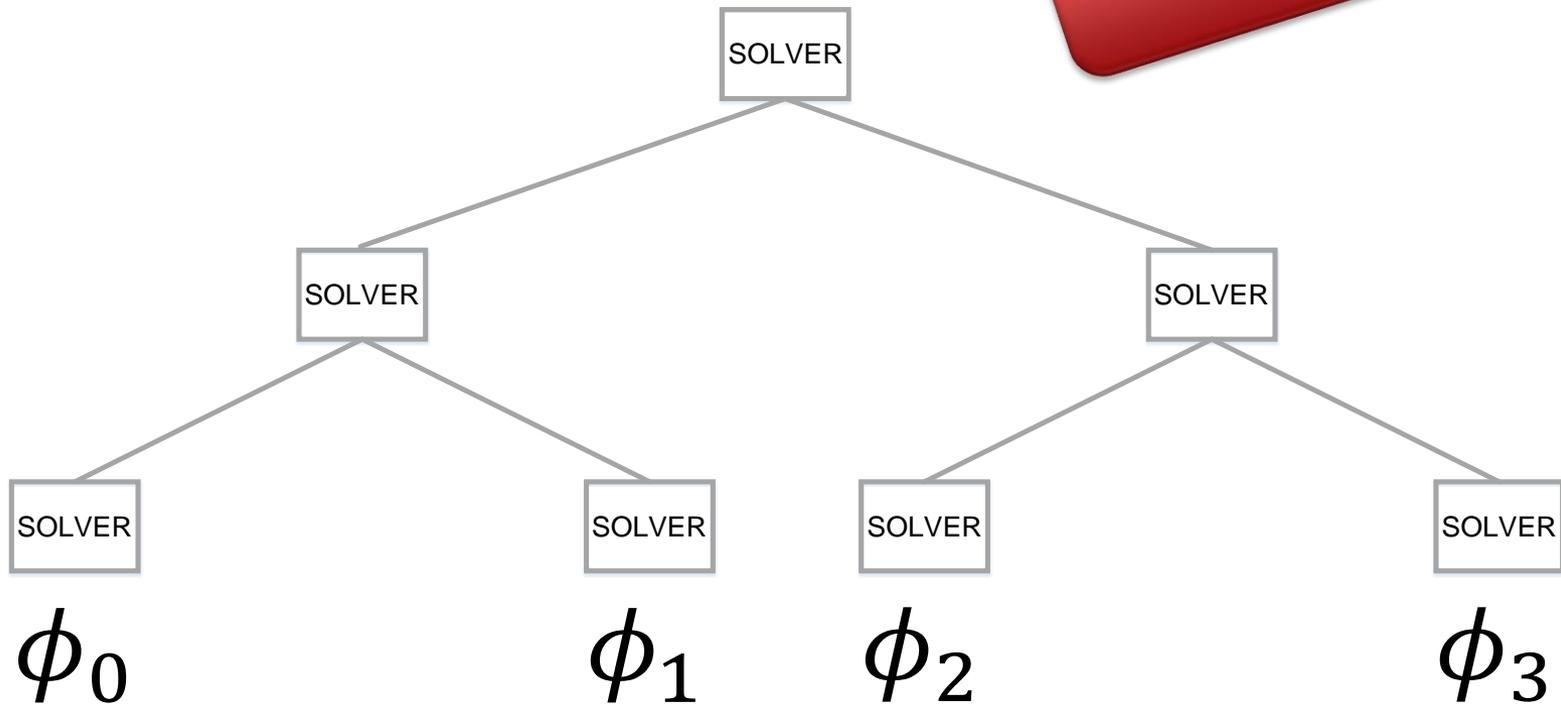
# Implementation

Input Partitions  $\phi_i$



# Implementation

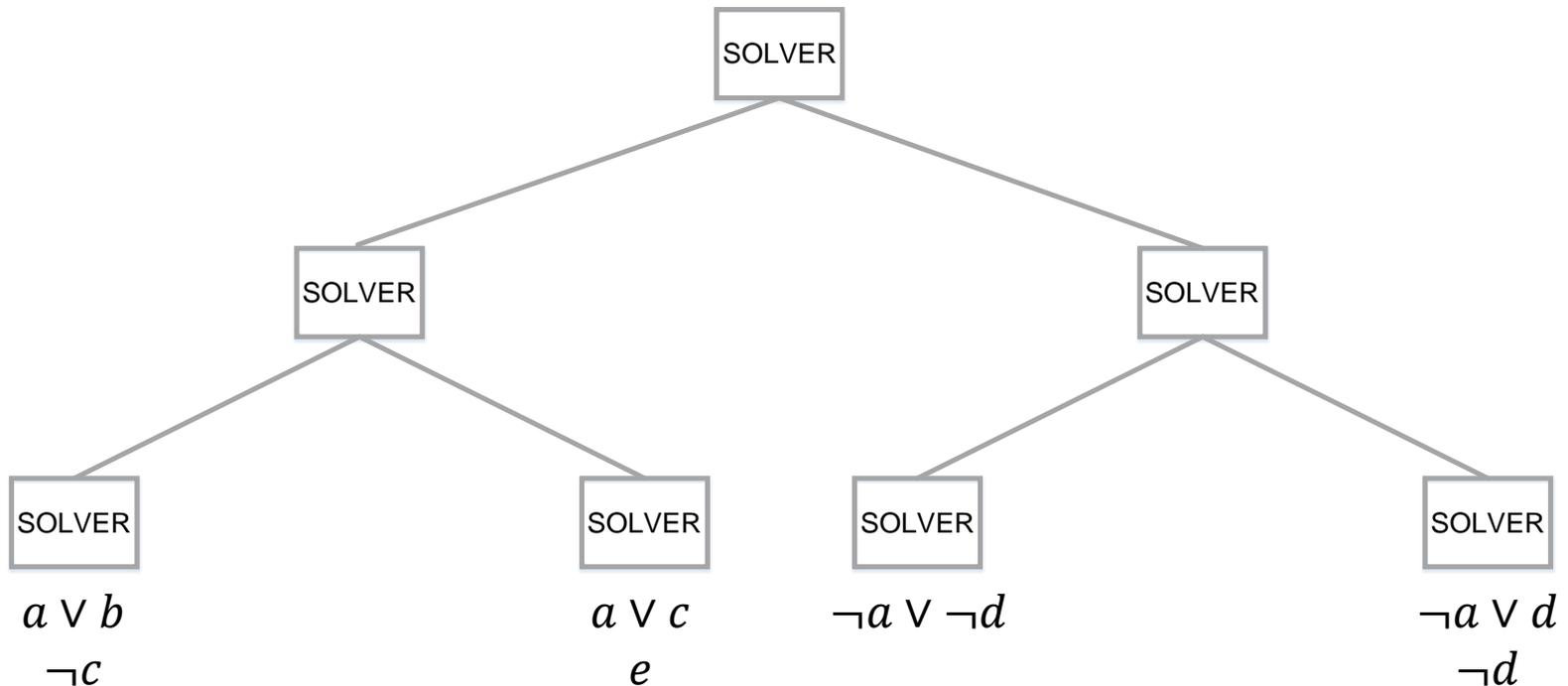
Extension of modular SAT  
Bayles et al., (FMCAD 2013)



Input Partitions  $\phi_i$

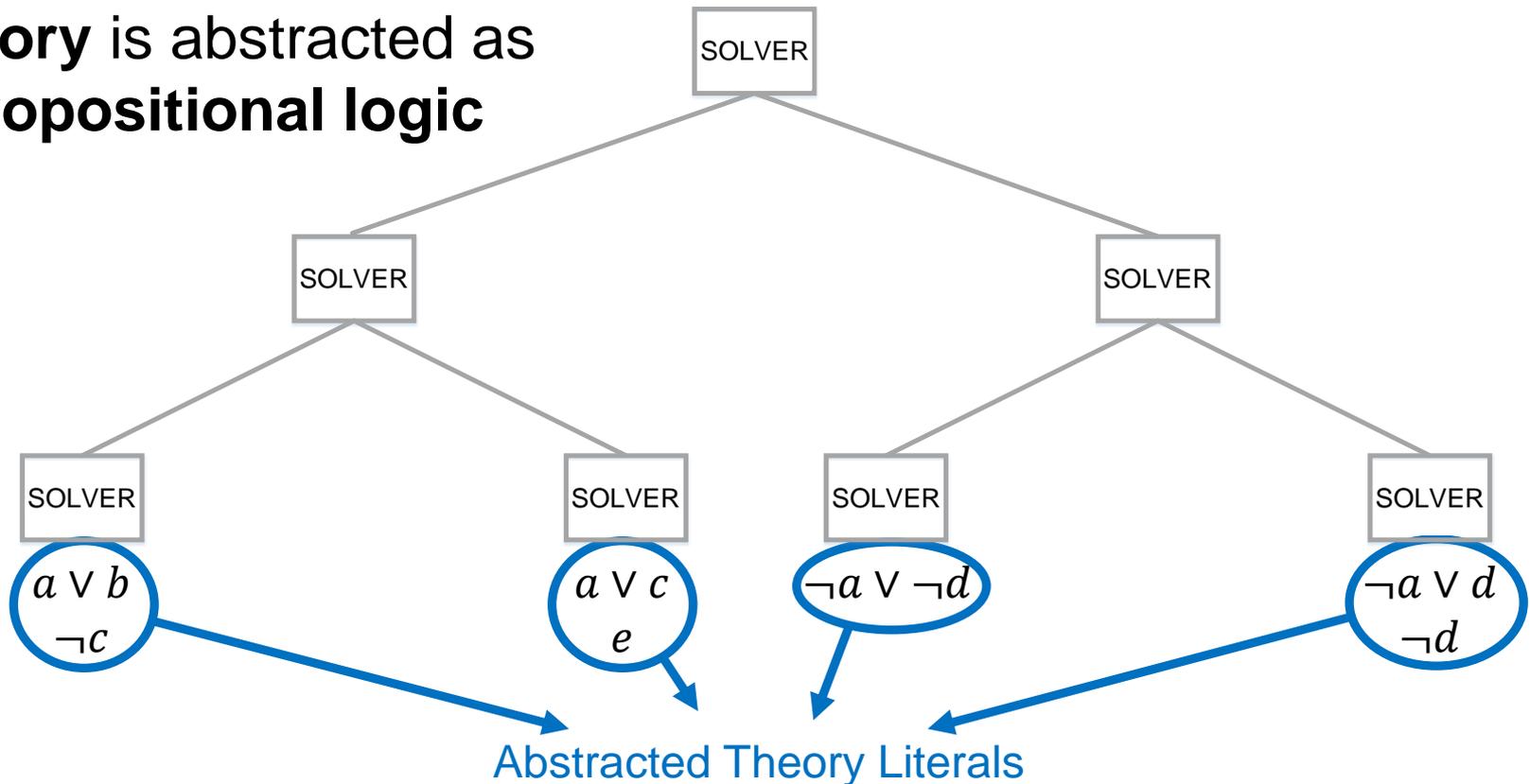
# Example

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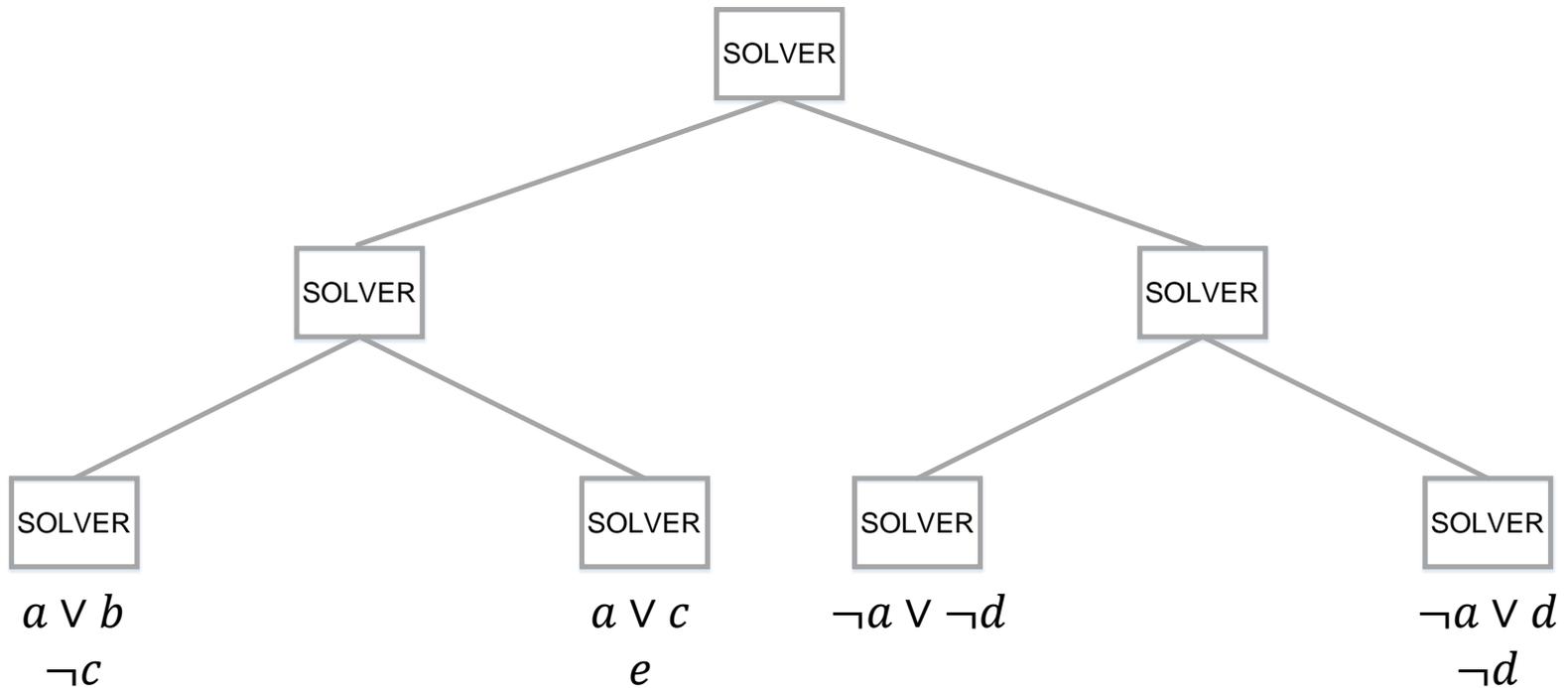


# Example

**Theory is abstracted as propositional logic**

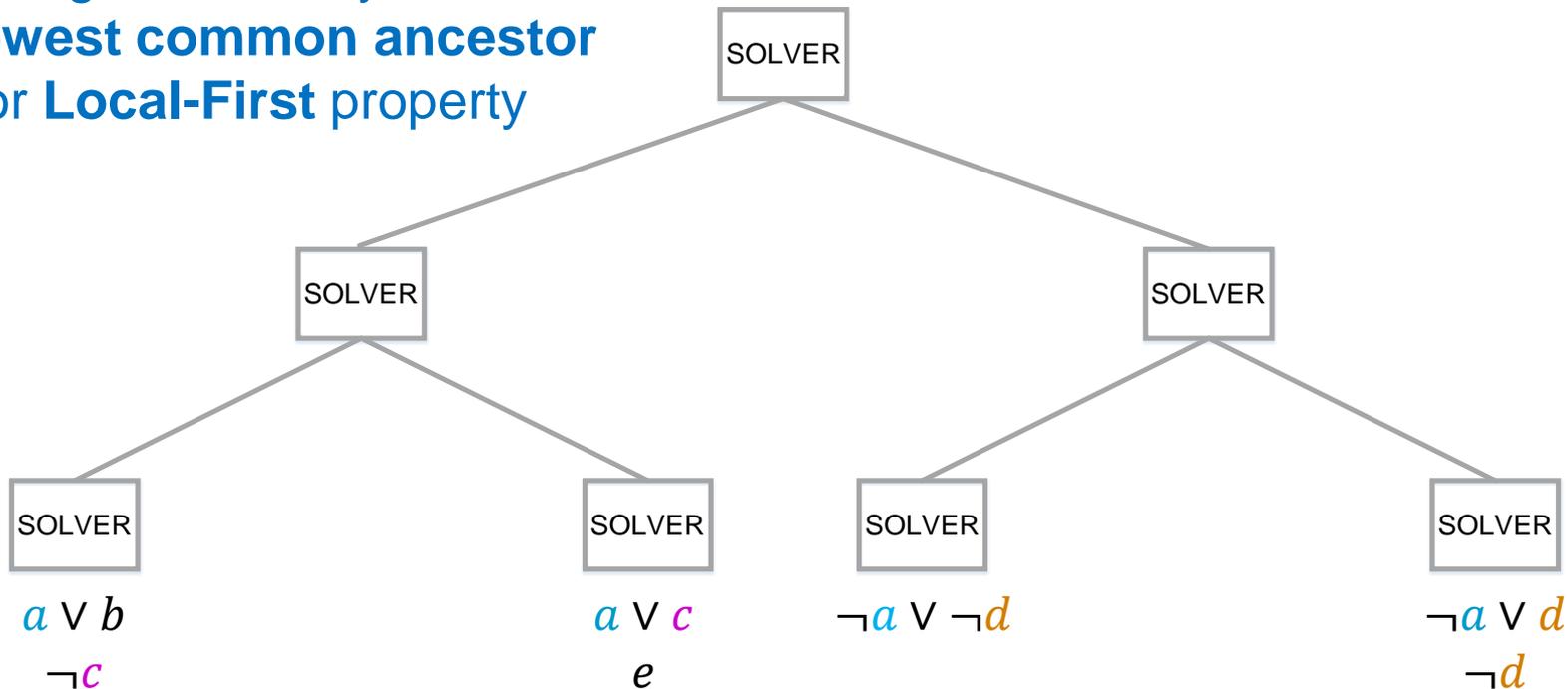


# Example



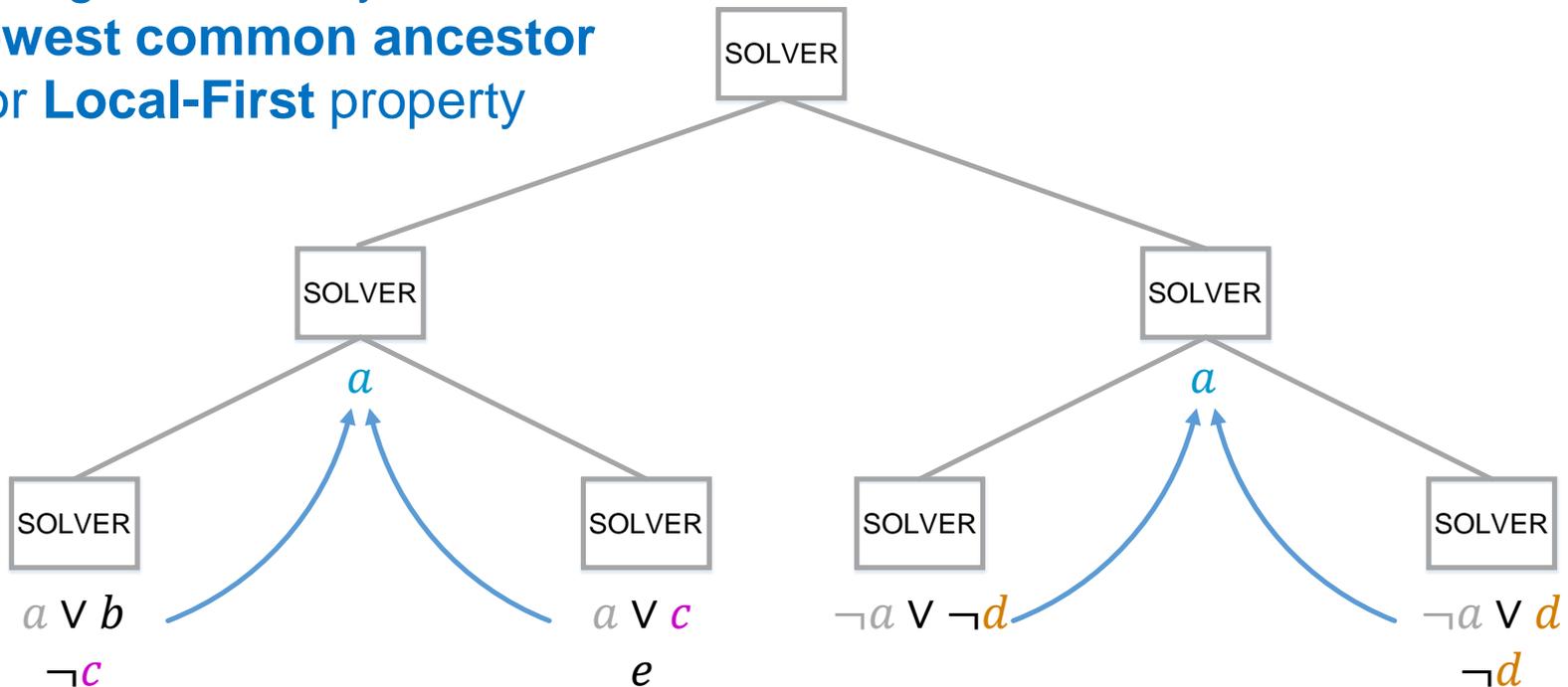
# Example

Assign **Global** Symbols  
to **lowest common ancestor**  
for **Local-First** property



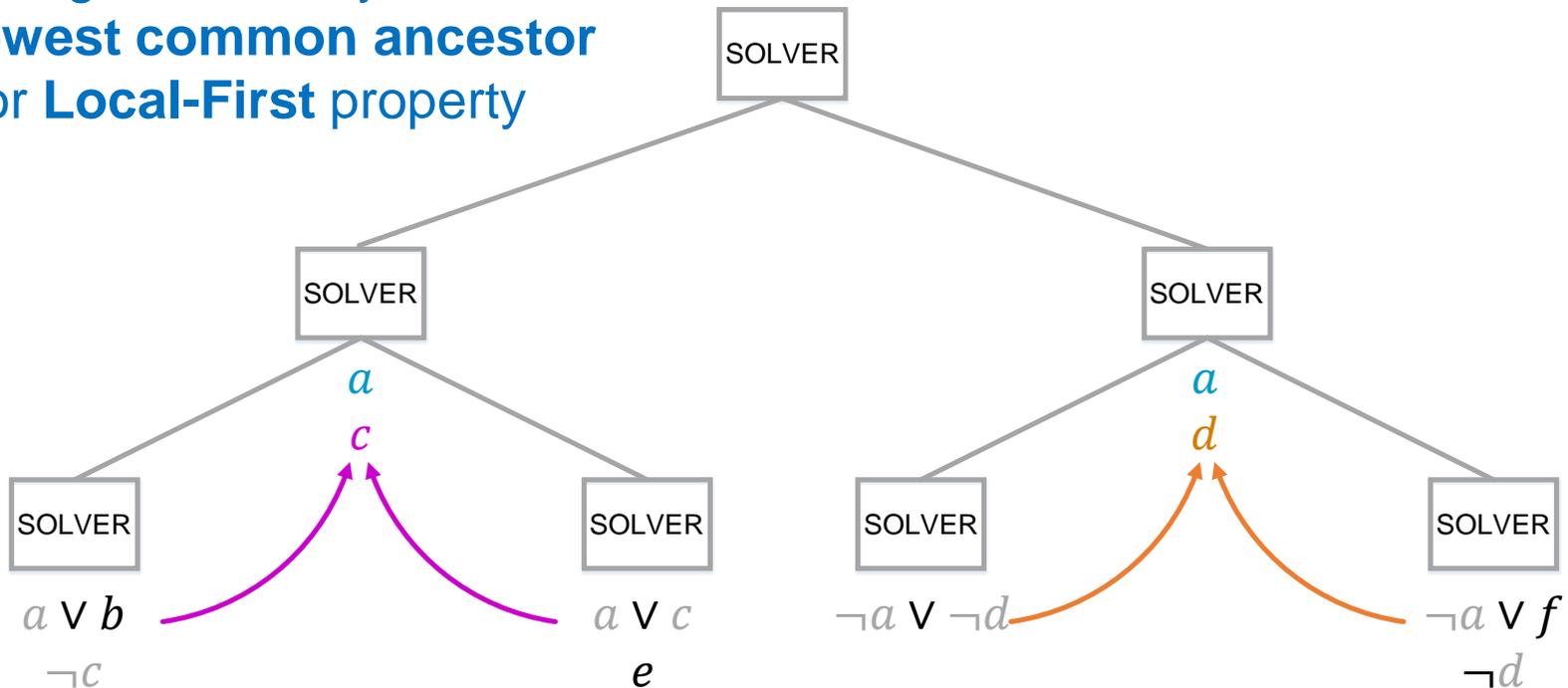
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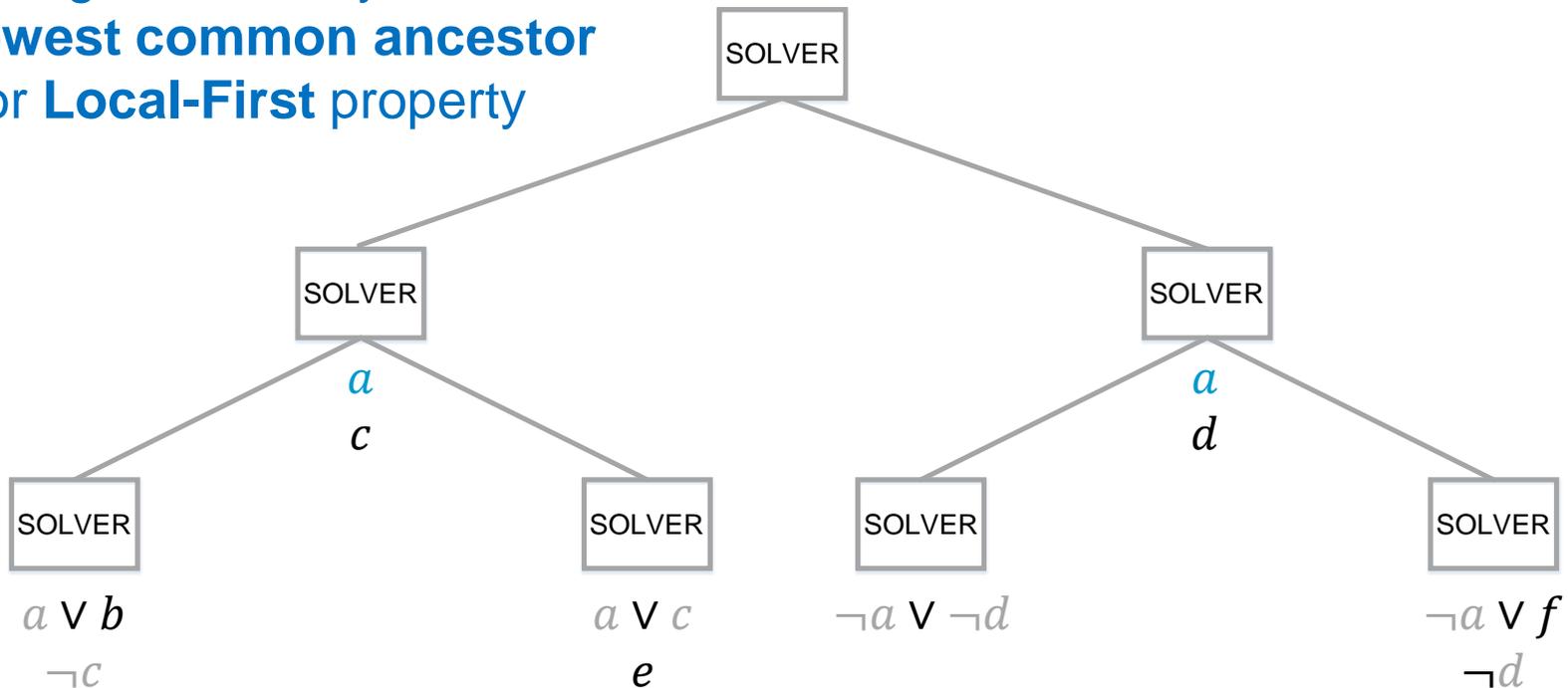
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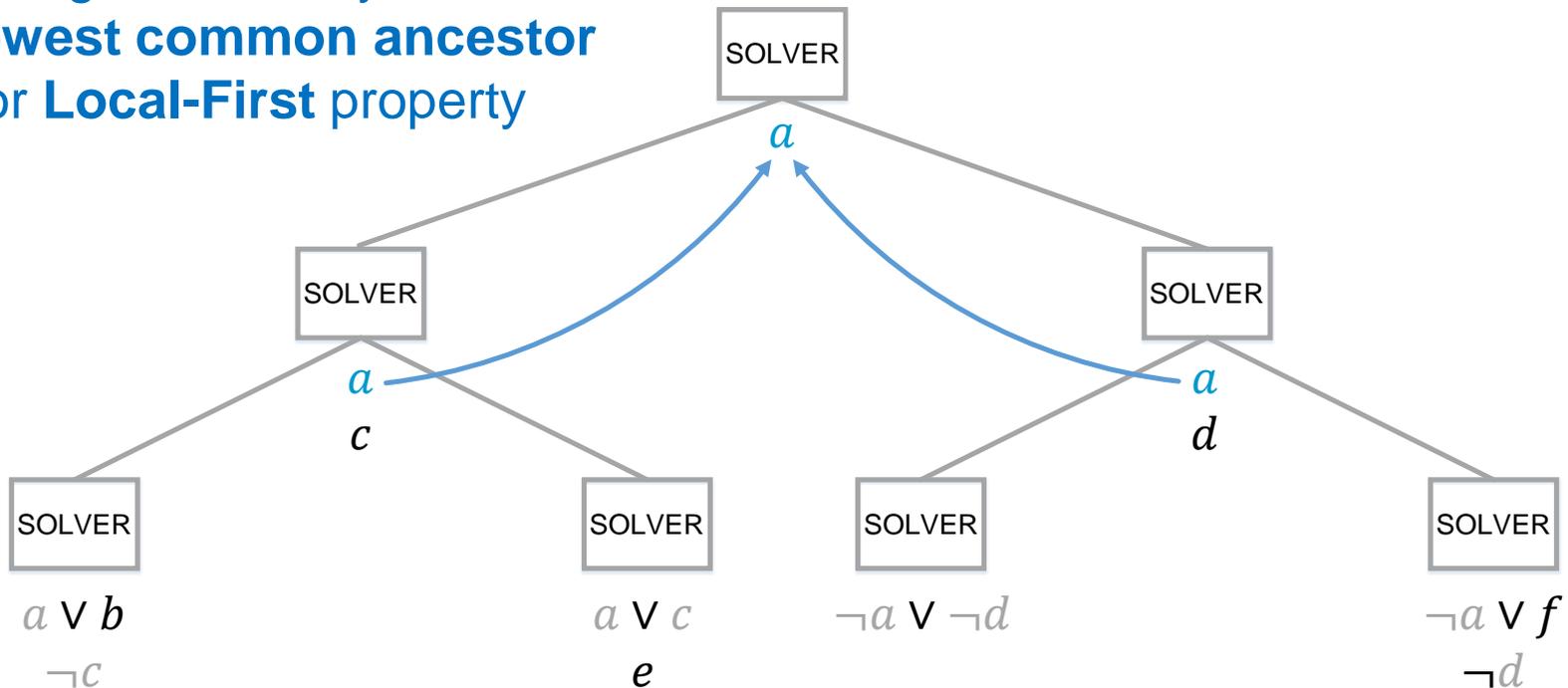
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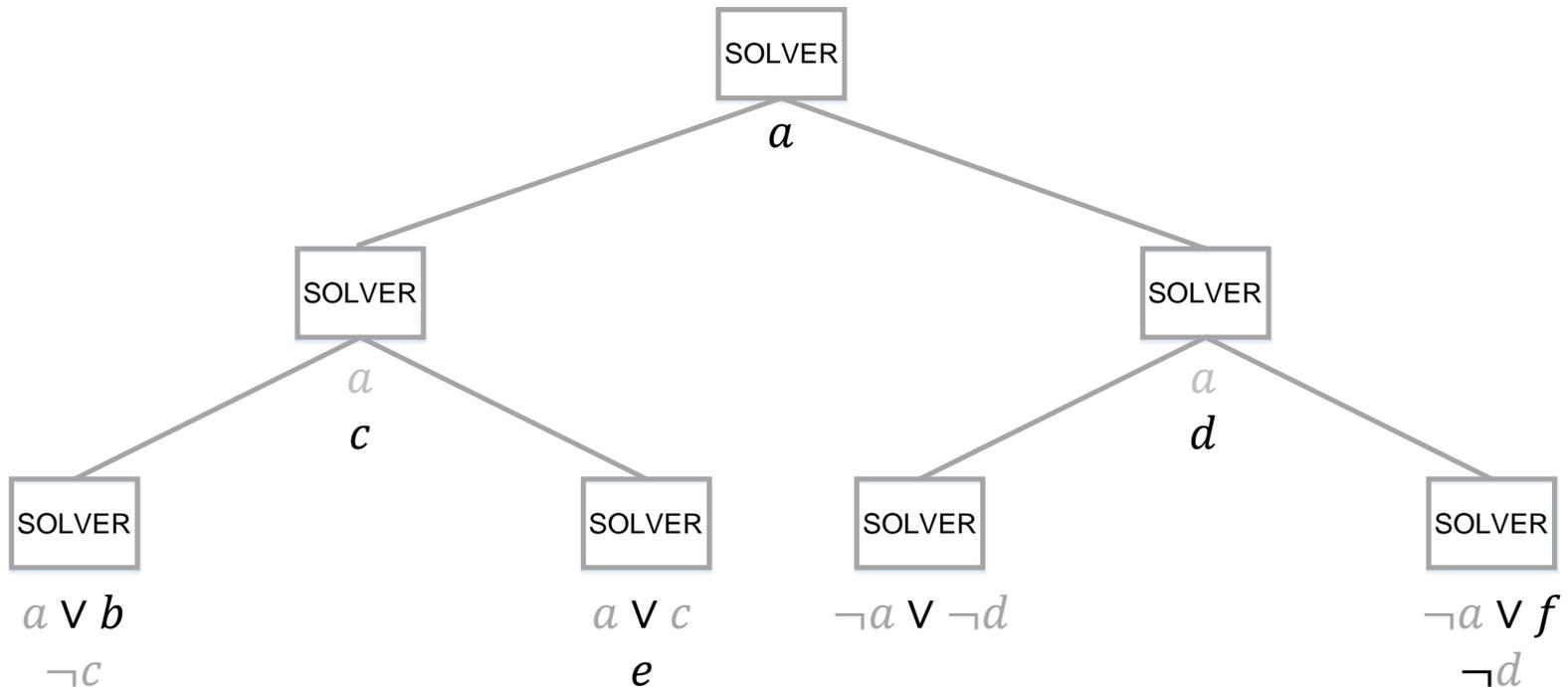


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Assign **Global** Symbols  
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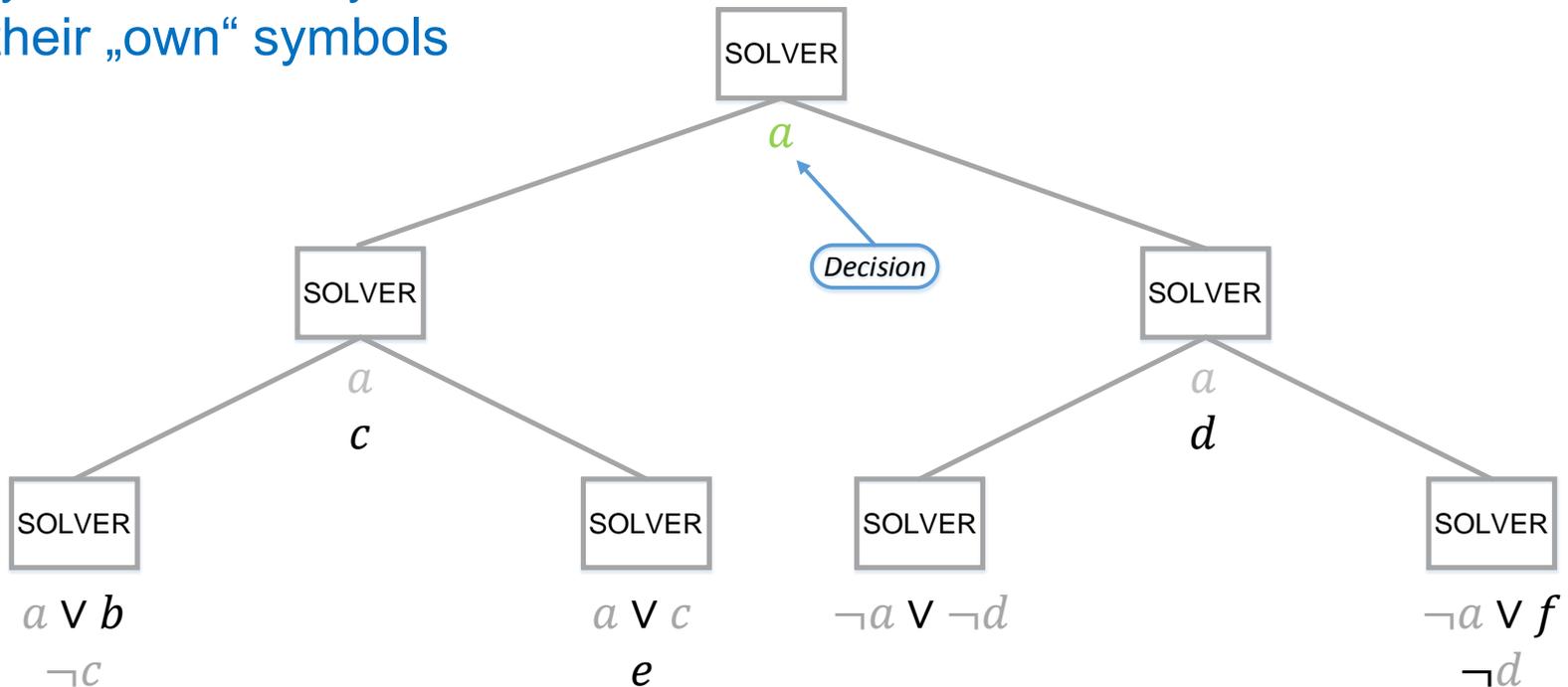


# Example



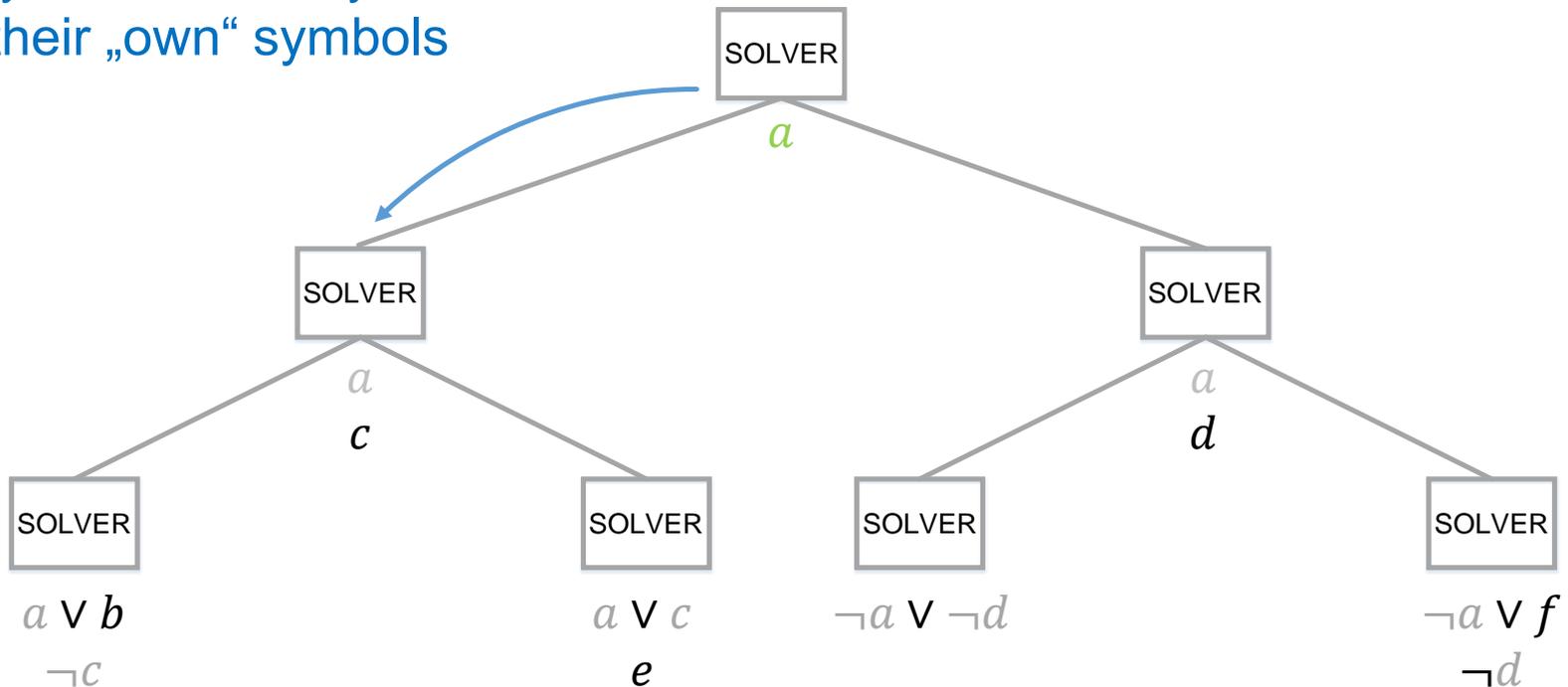
# Example

Every node can only decide their „own“ symbols



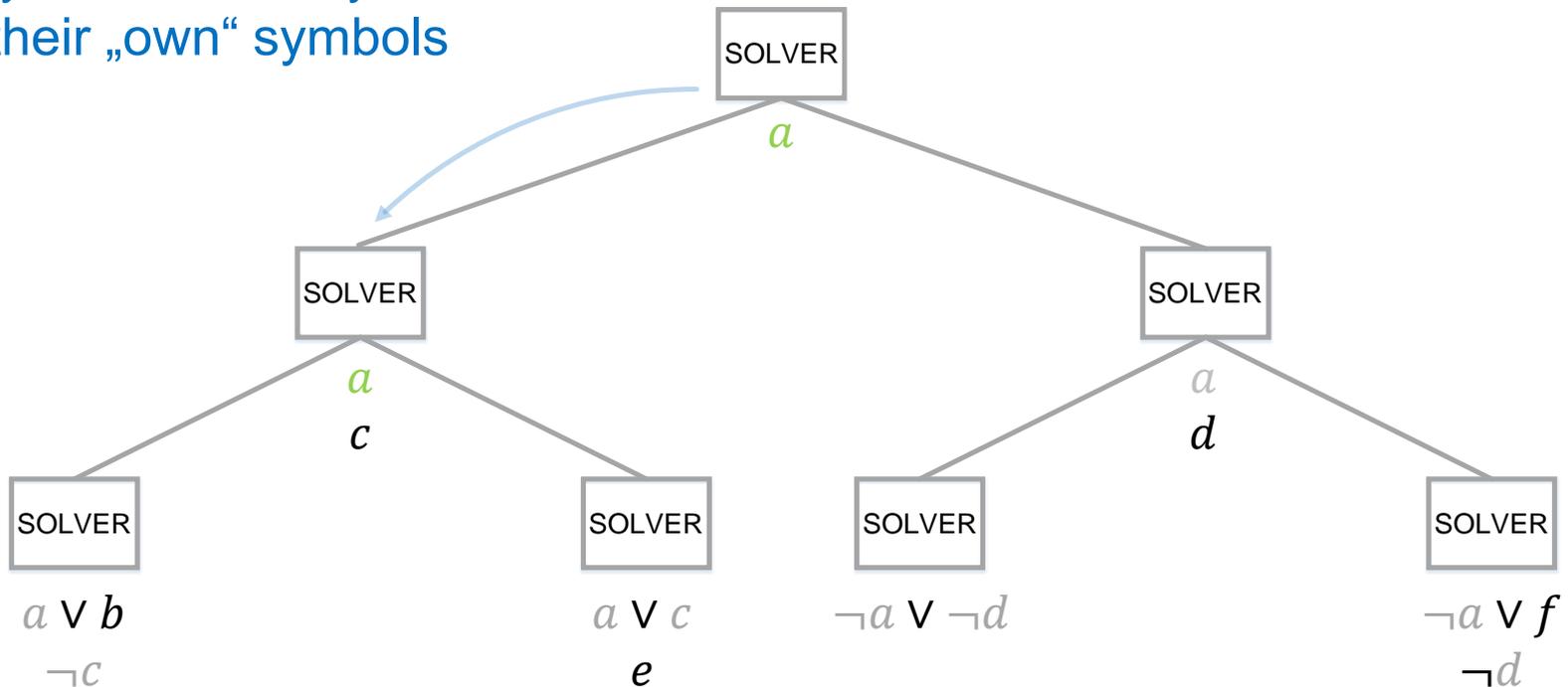
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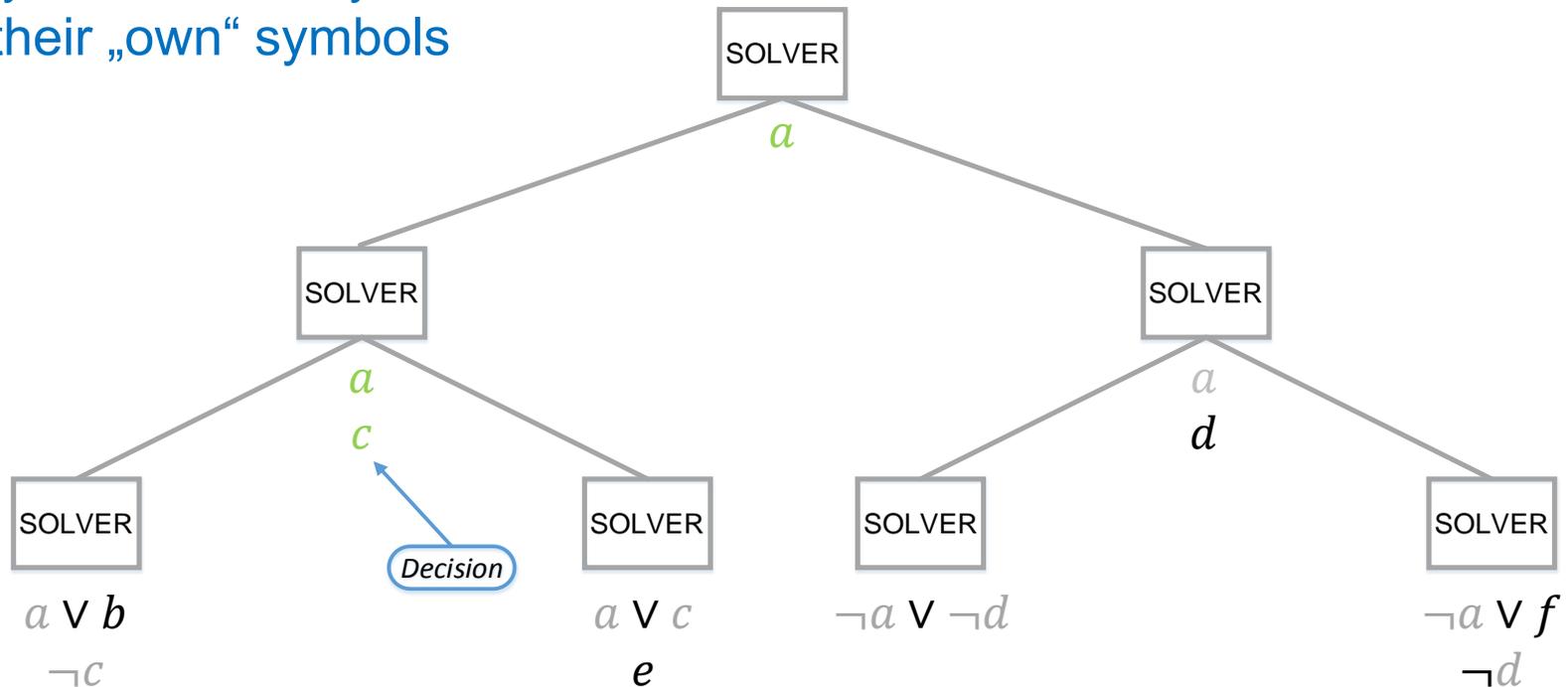
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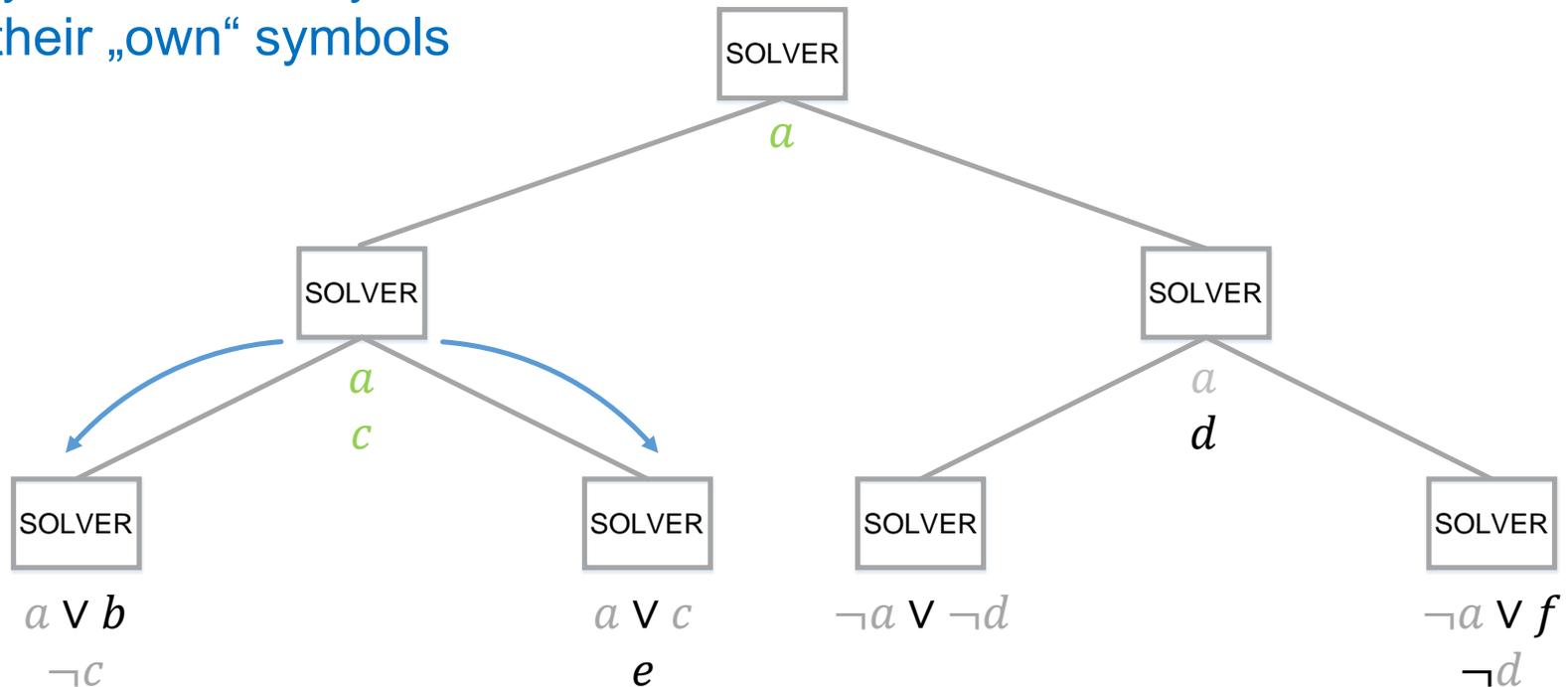
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Every node can only decide their „own“ symbols



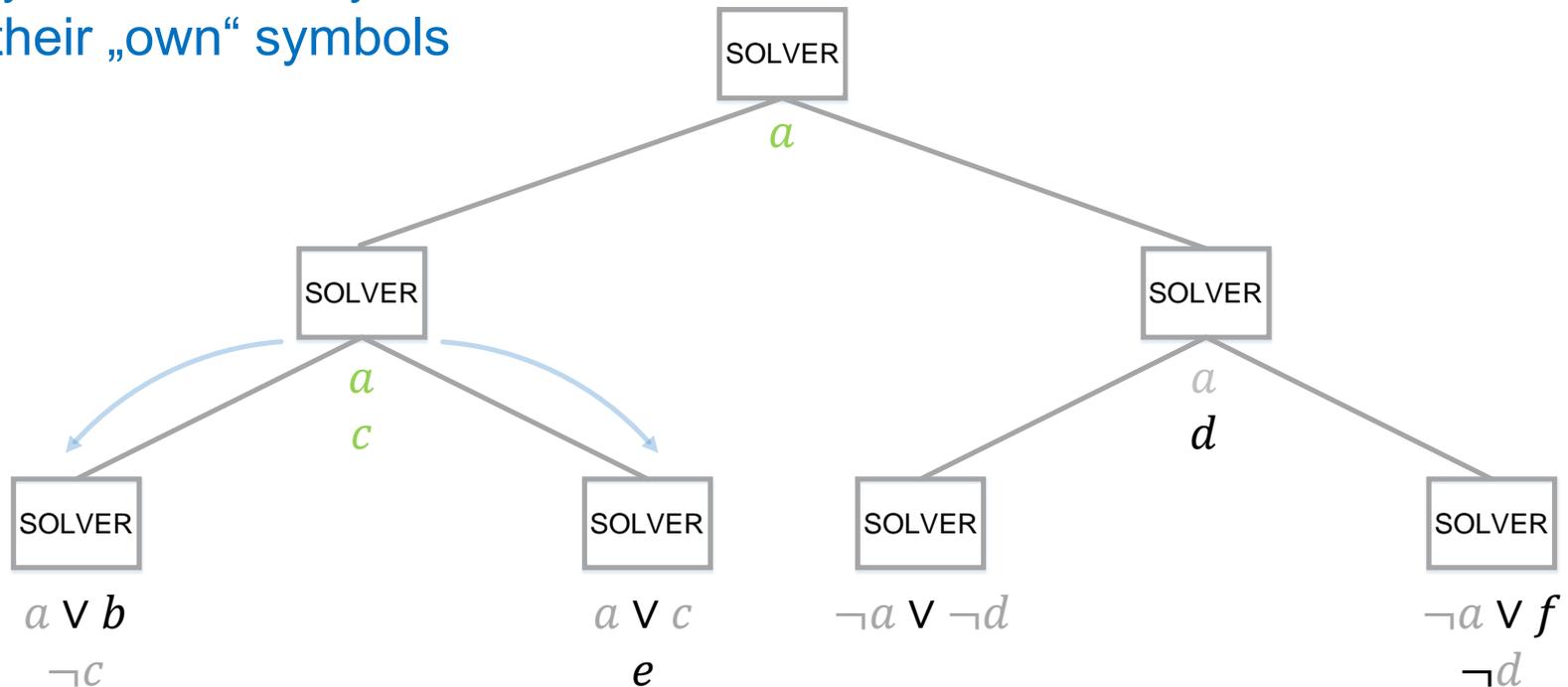
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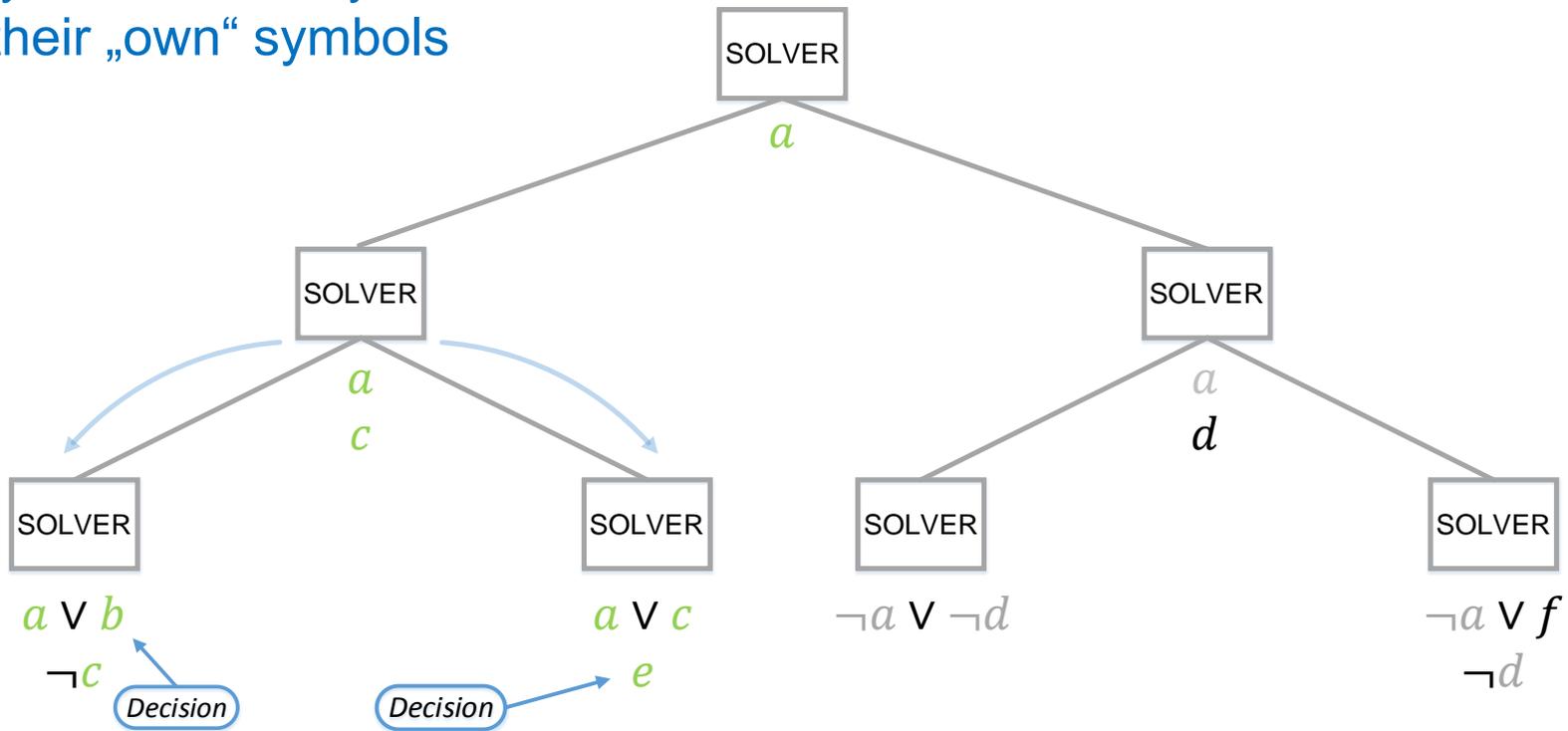
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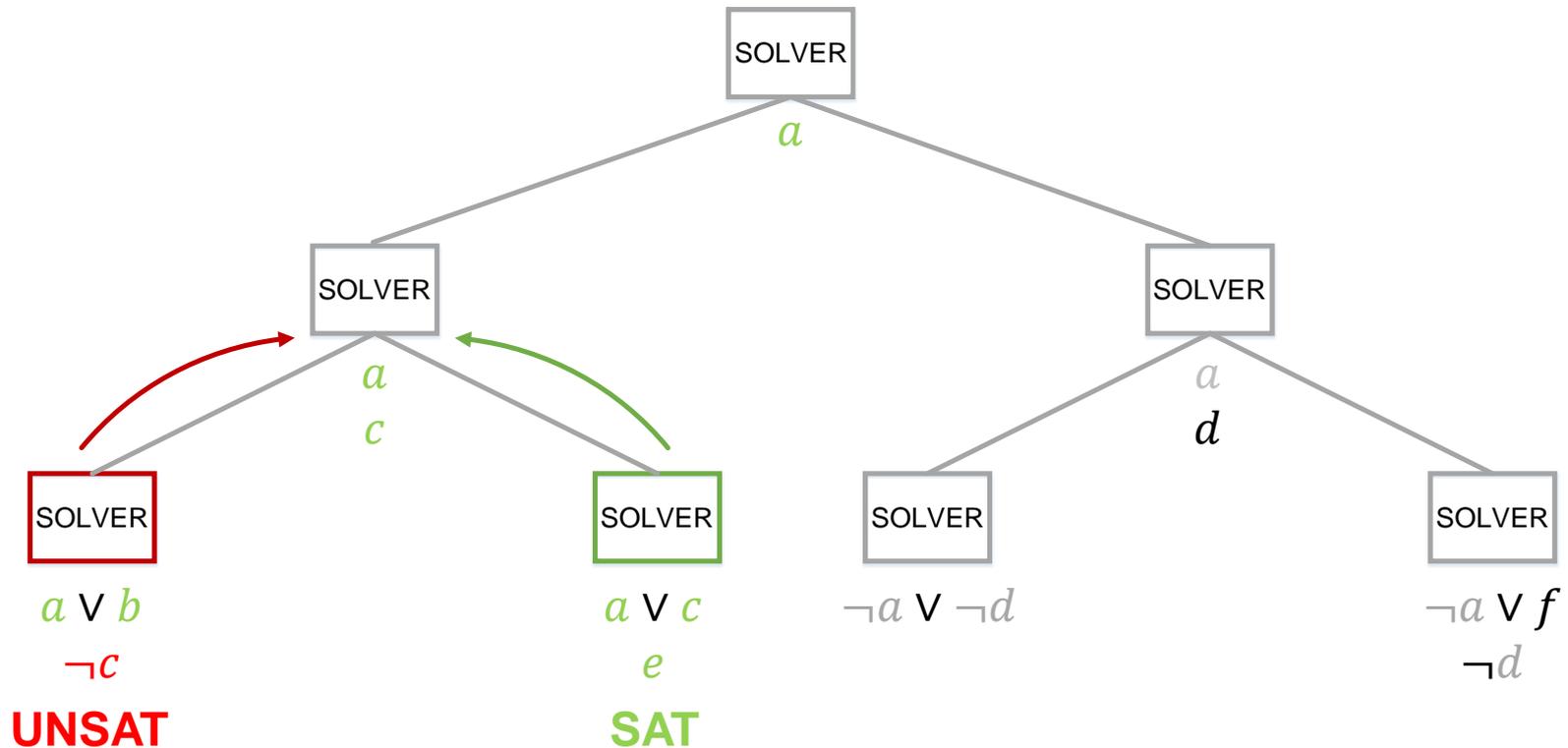


# Example

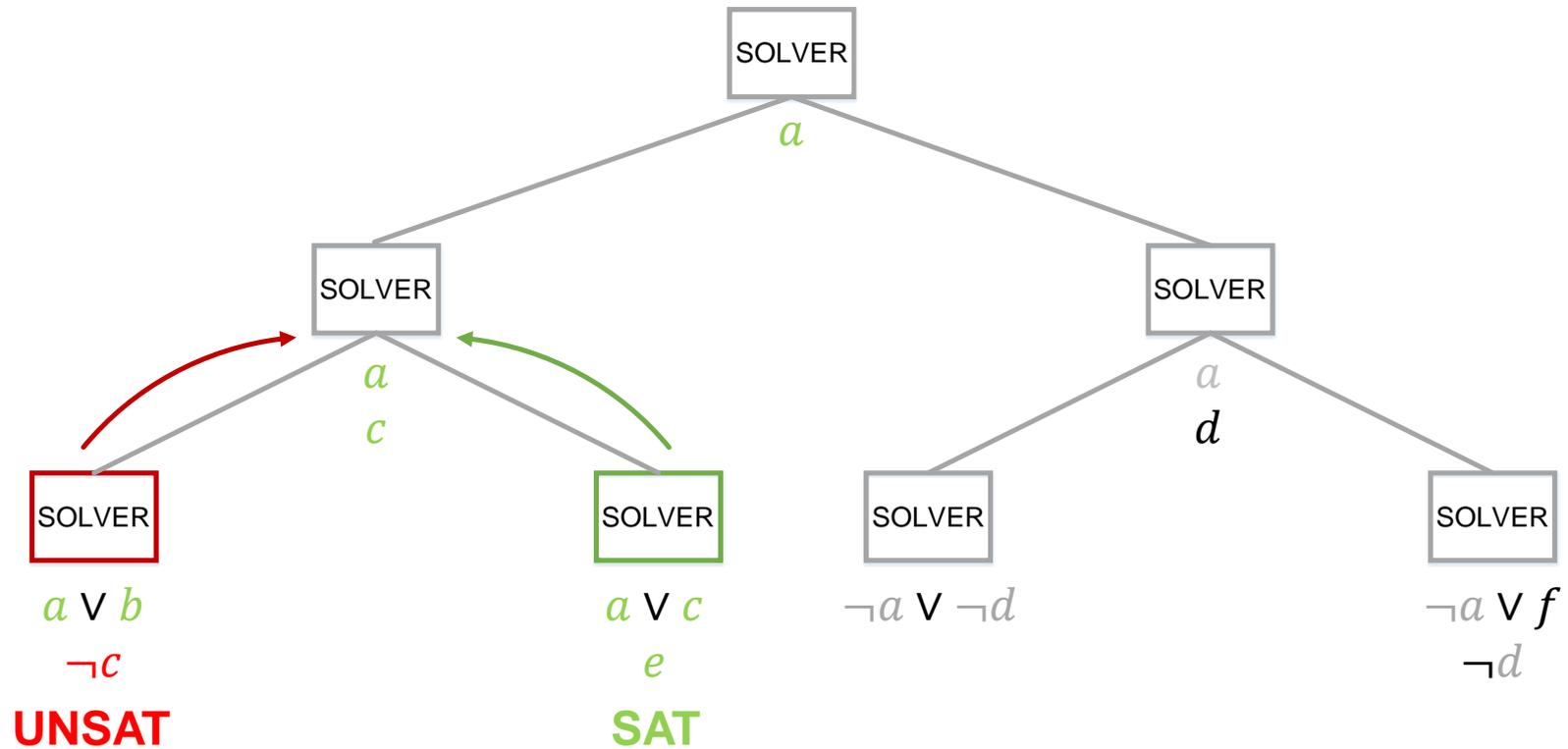
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# Example

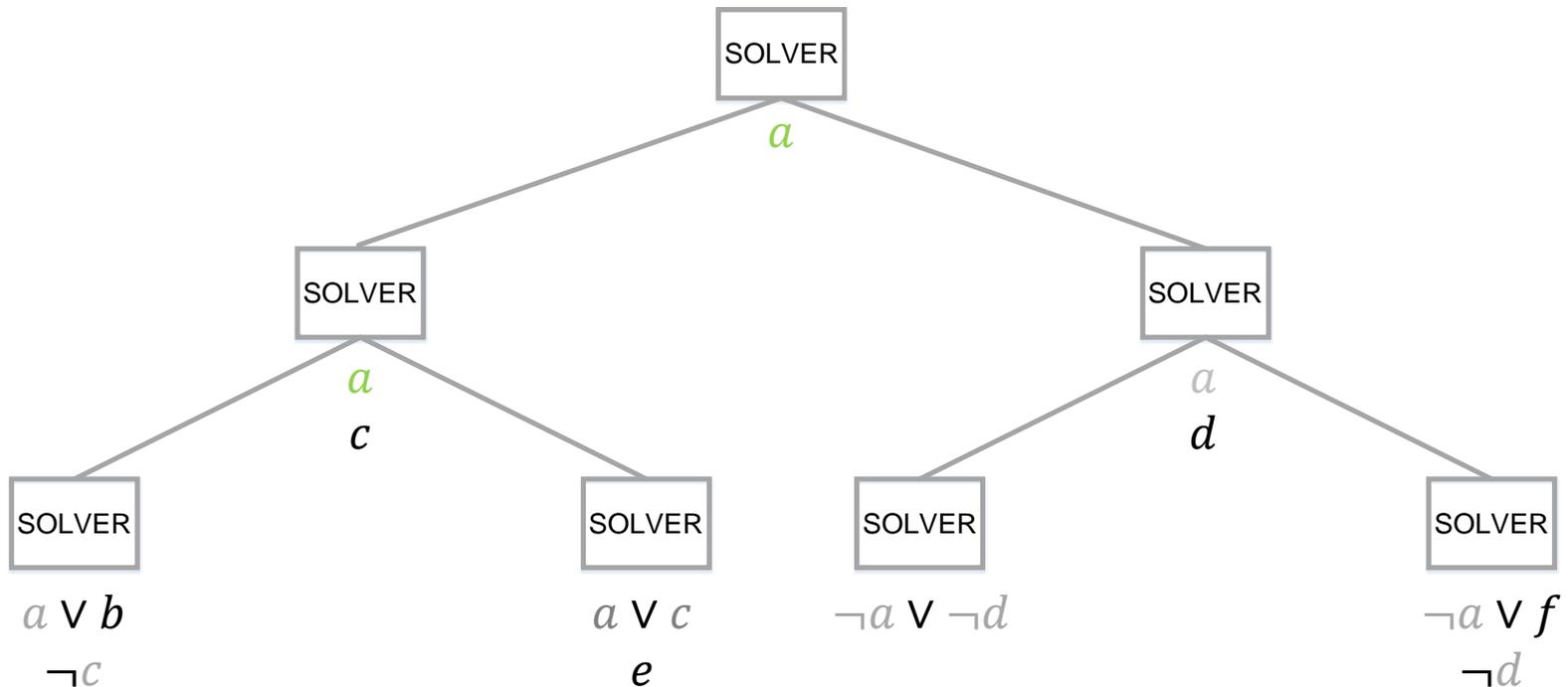


# Example

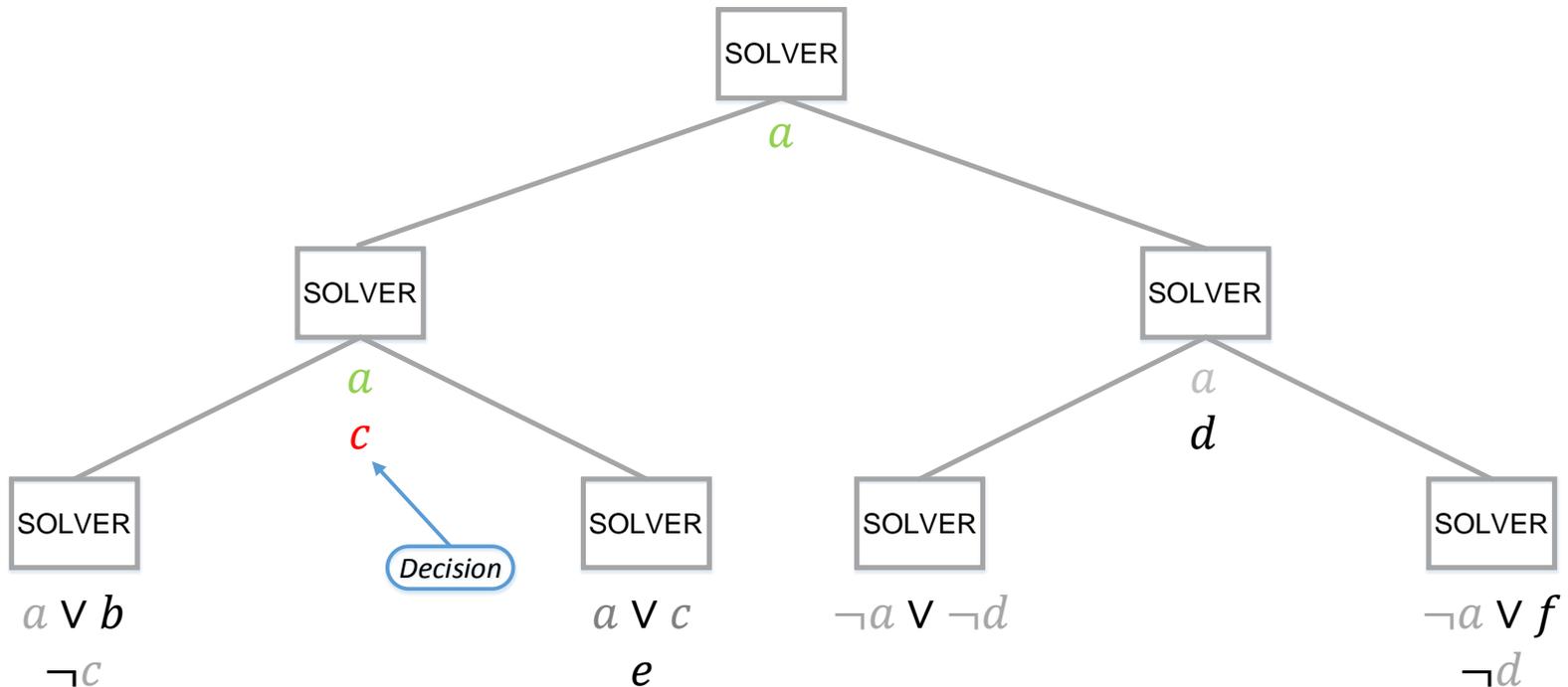




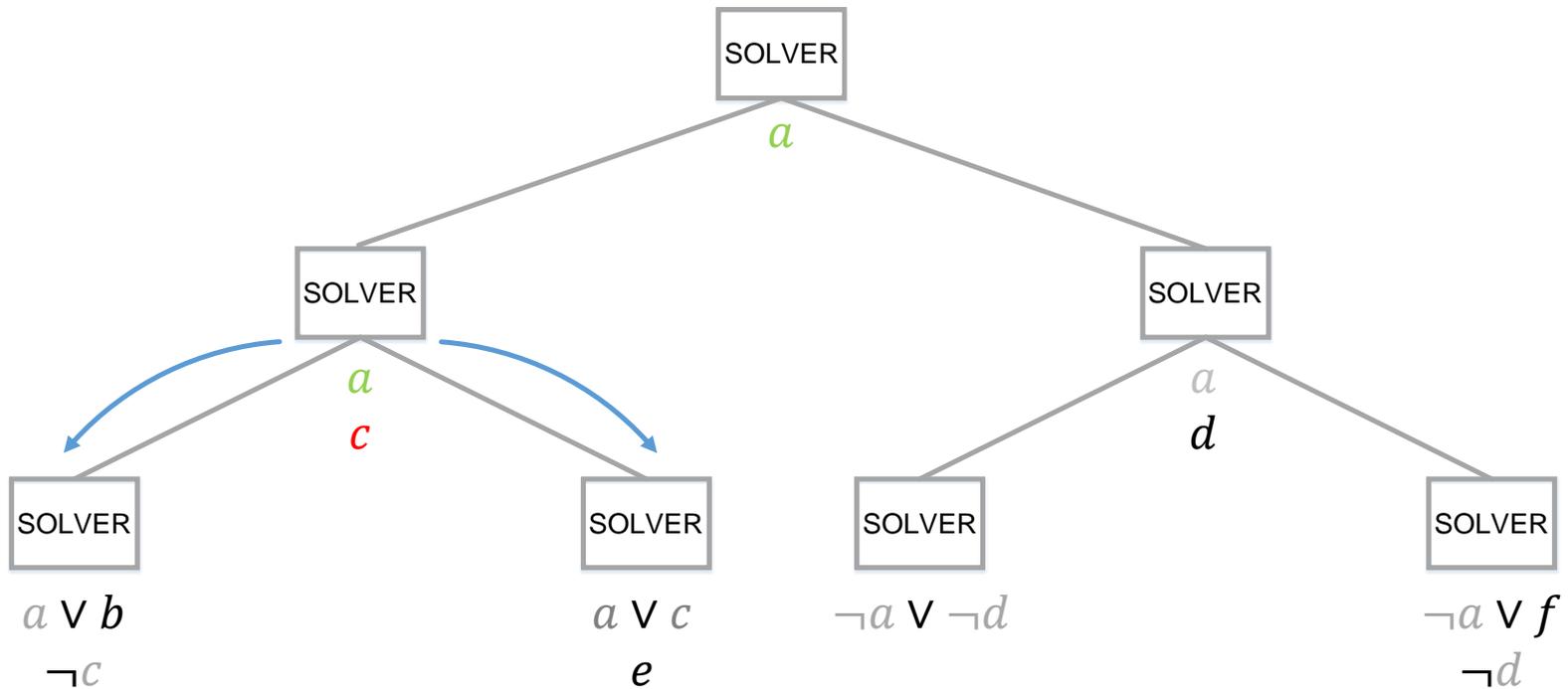
# Example



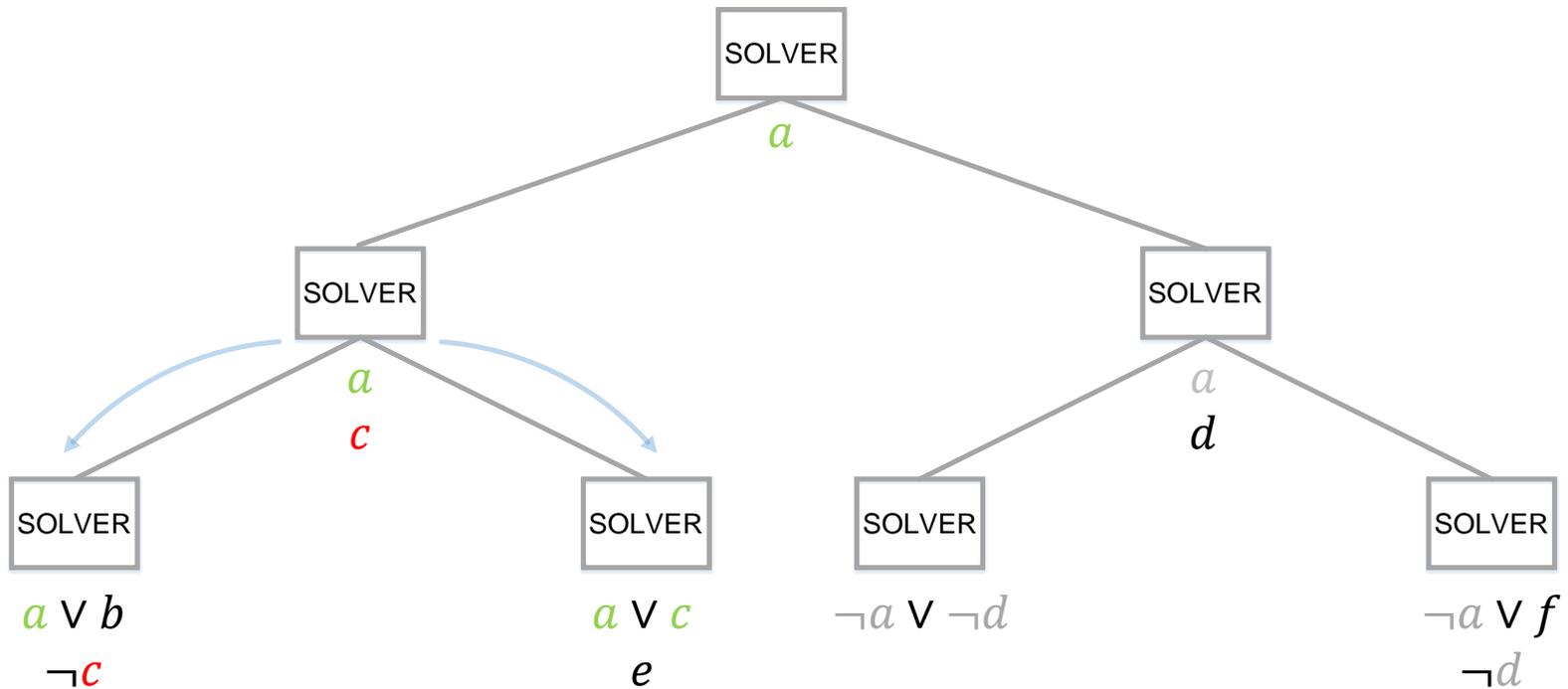
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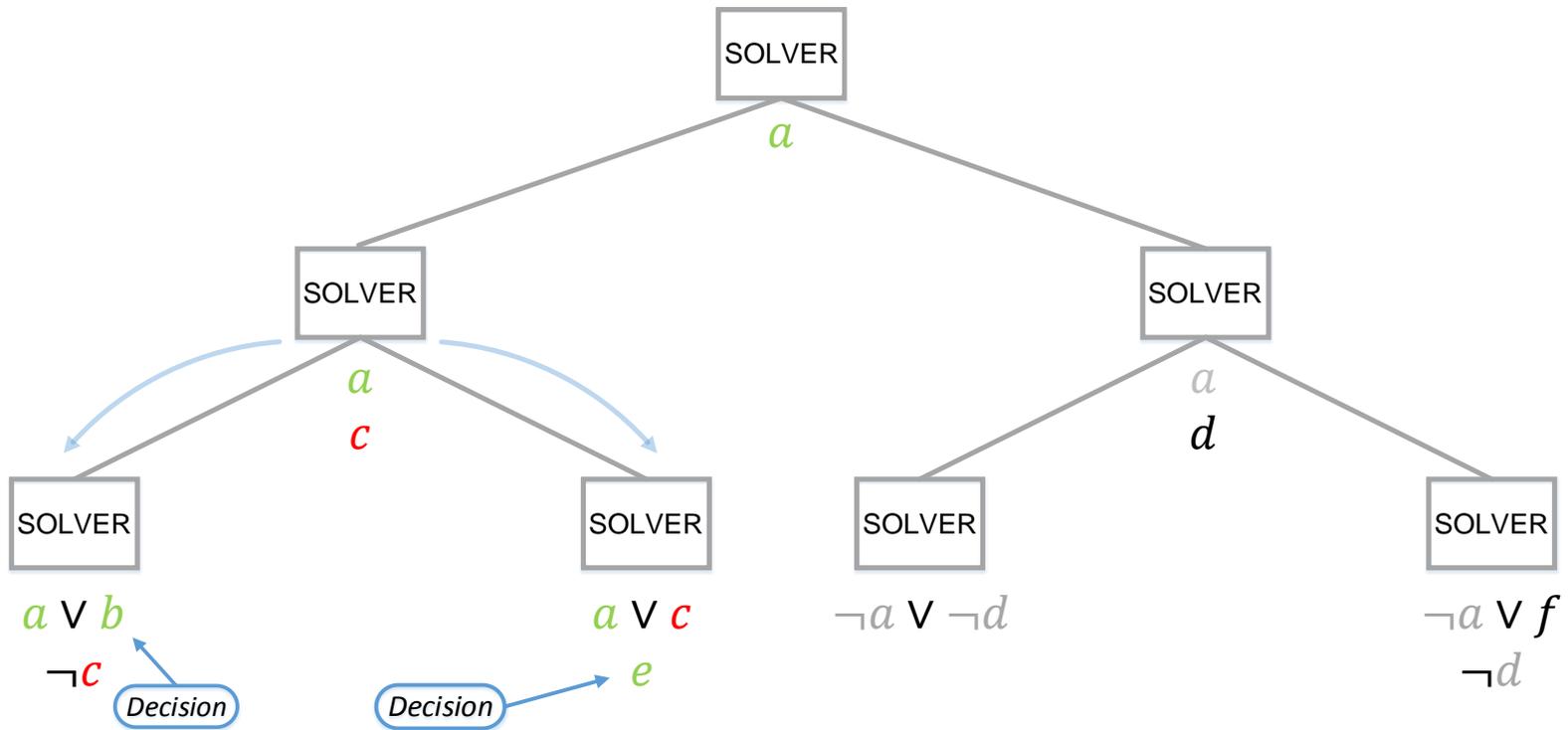
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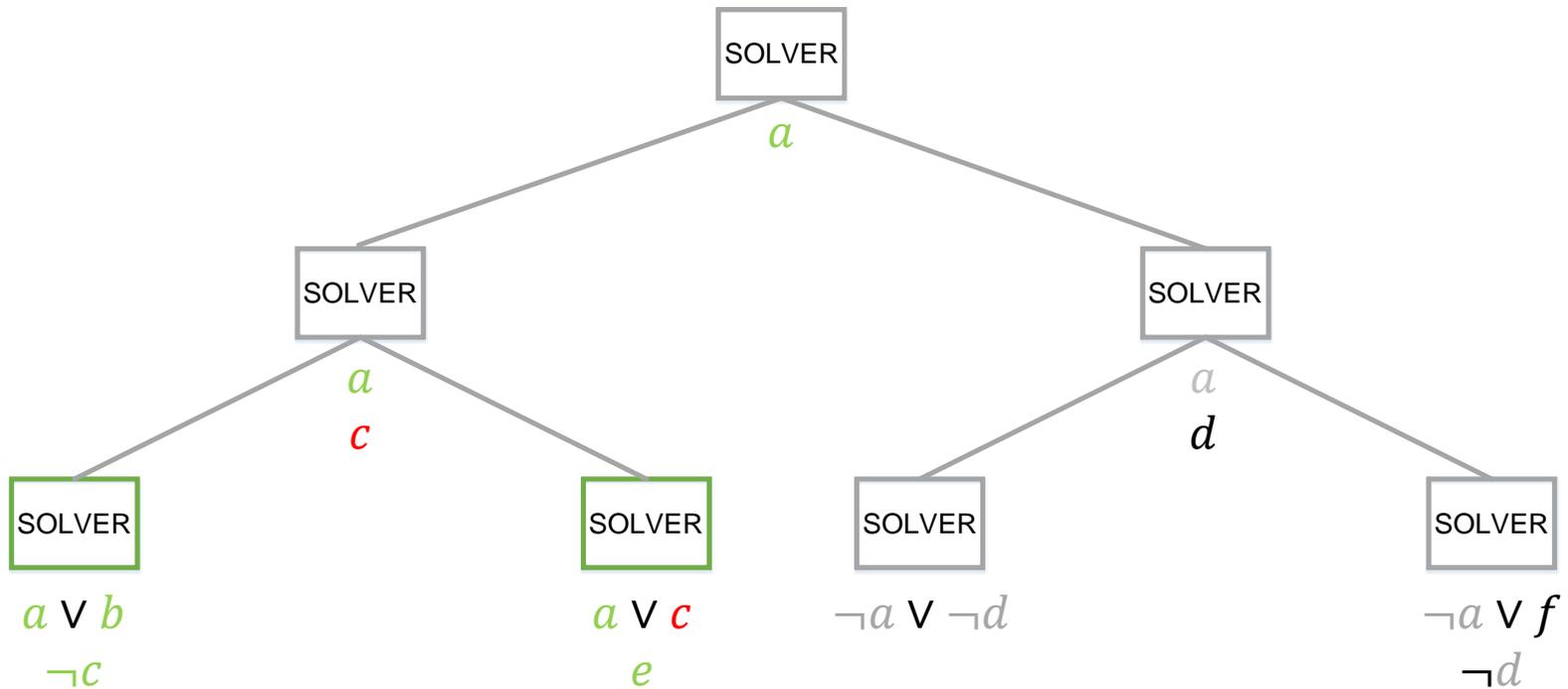
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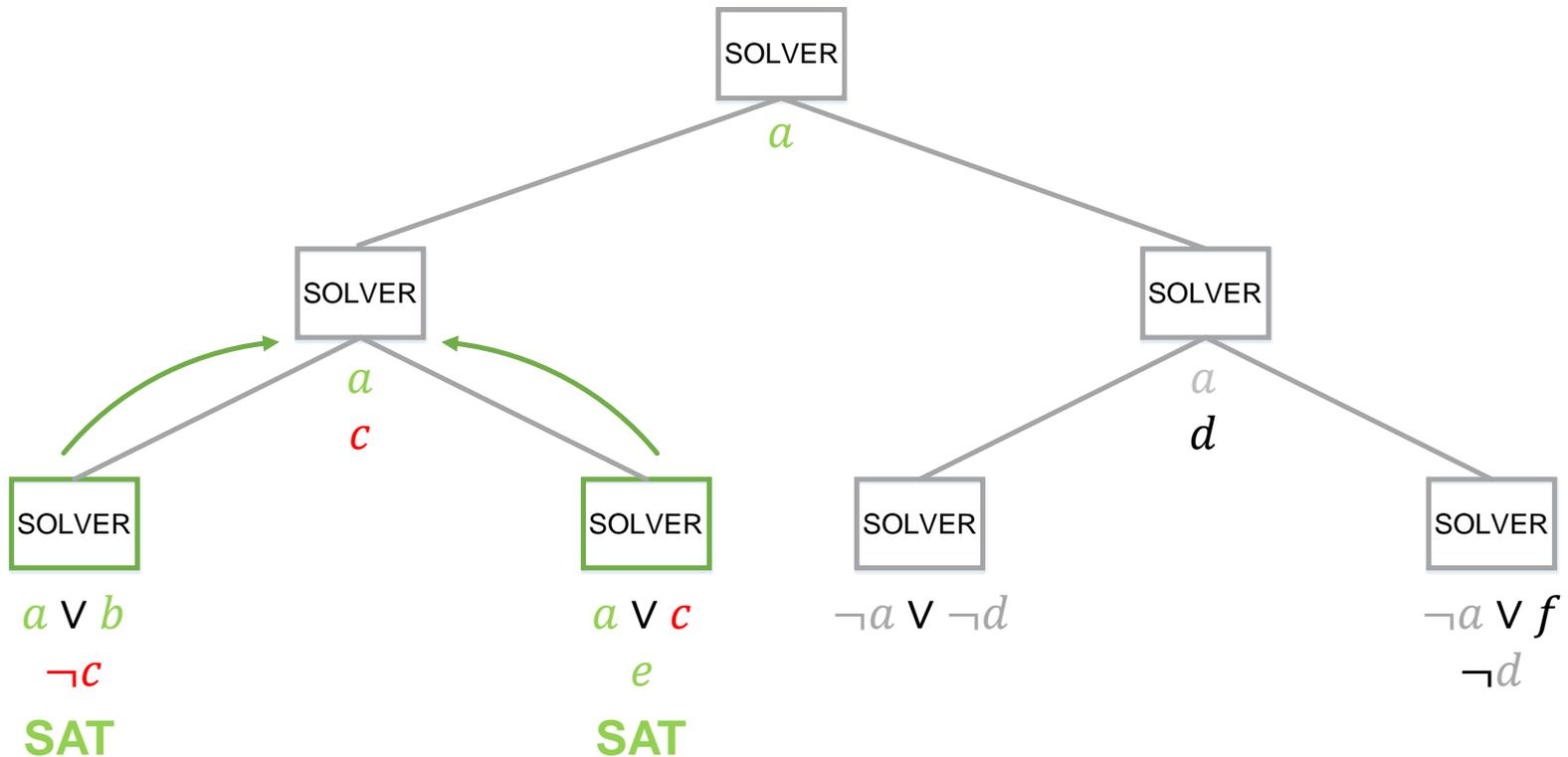
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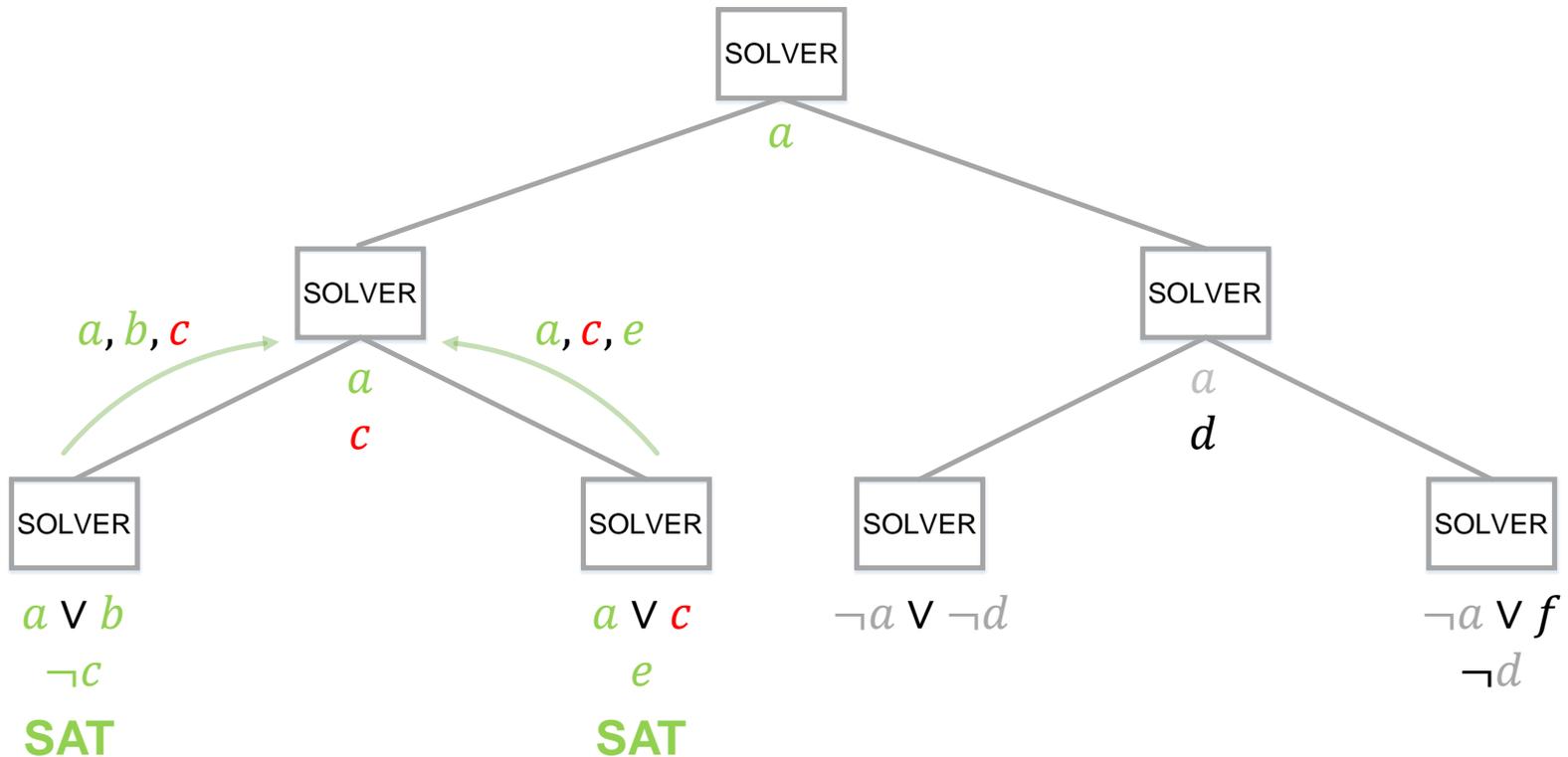
# Example



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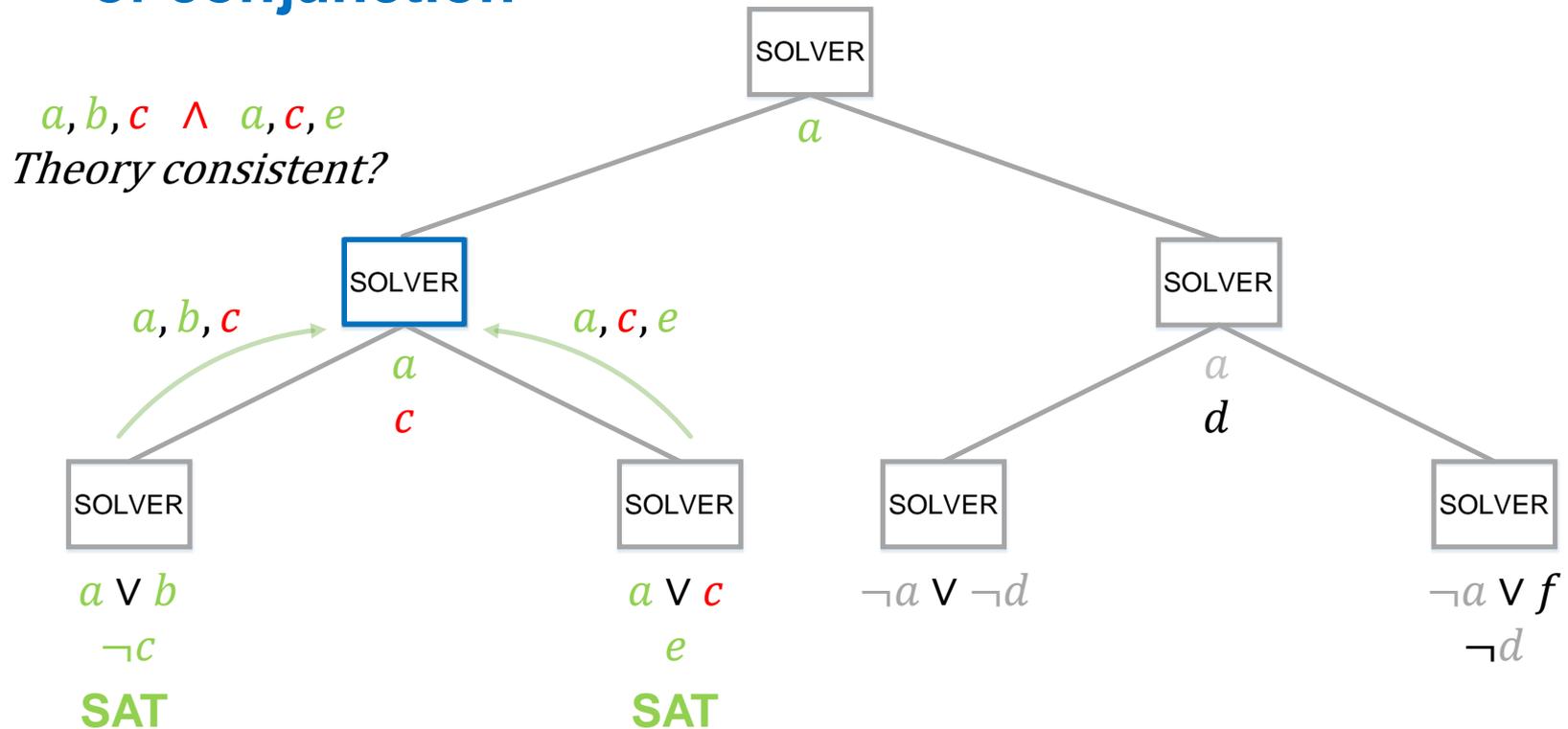


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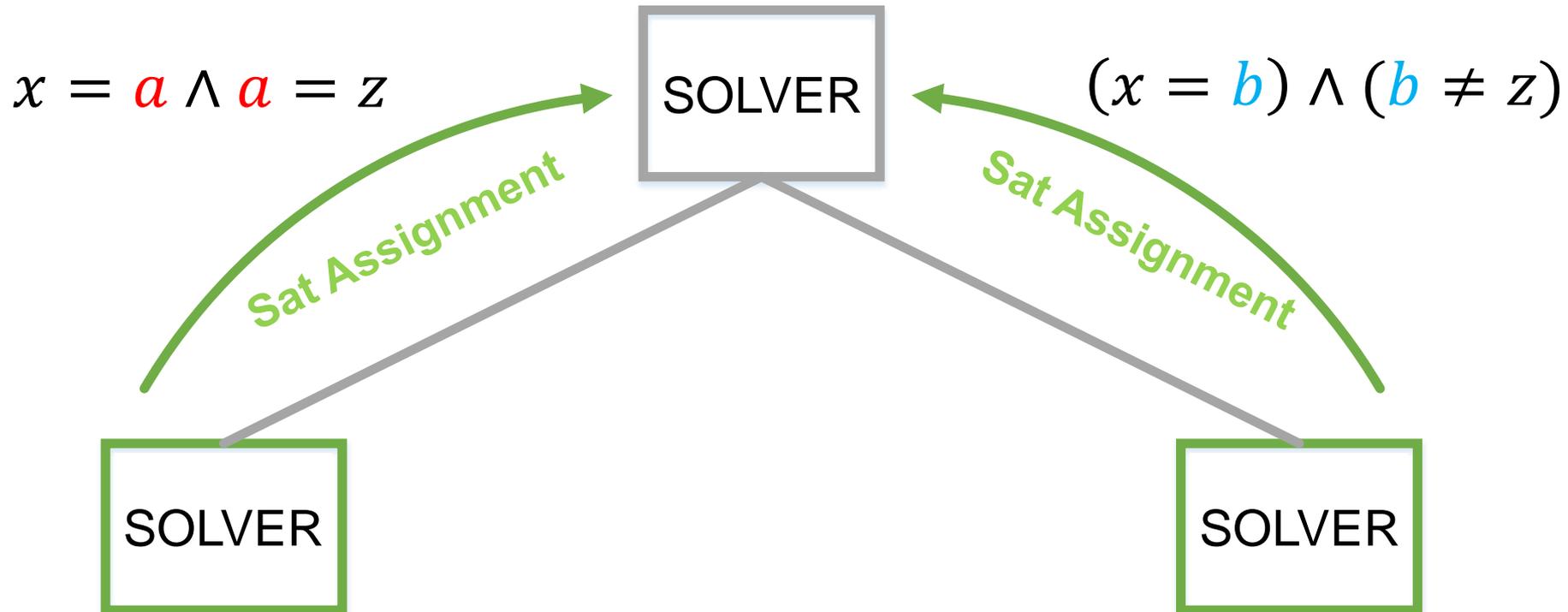


# Example

## Theory check of conjunction

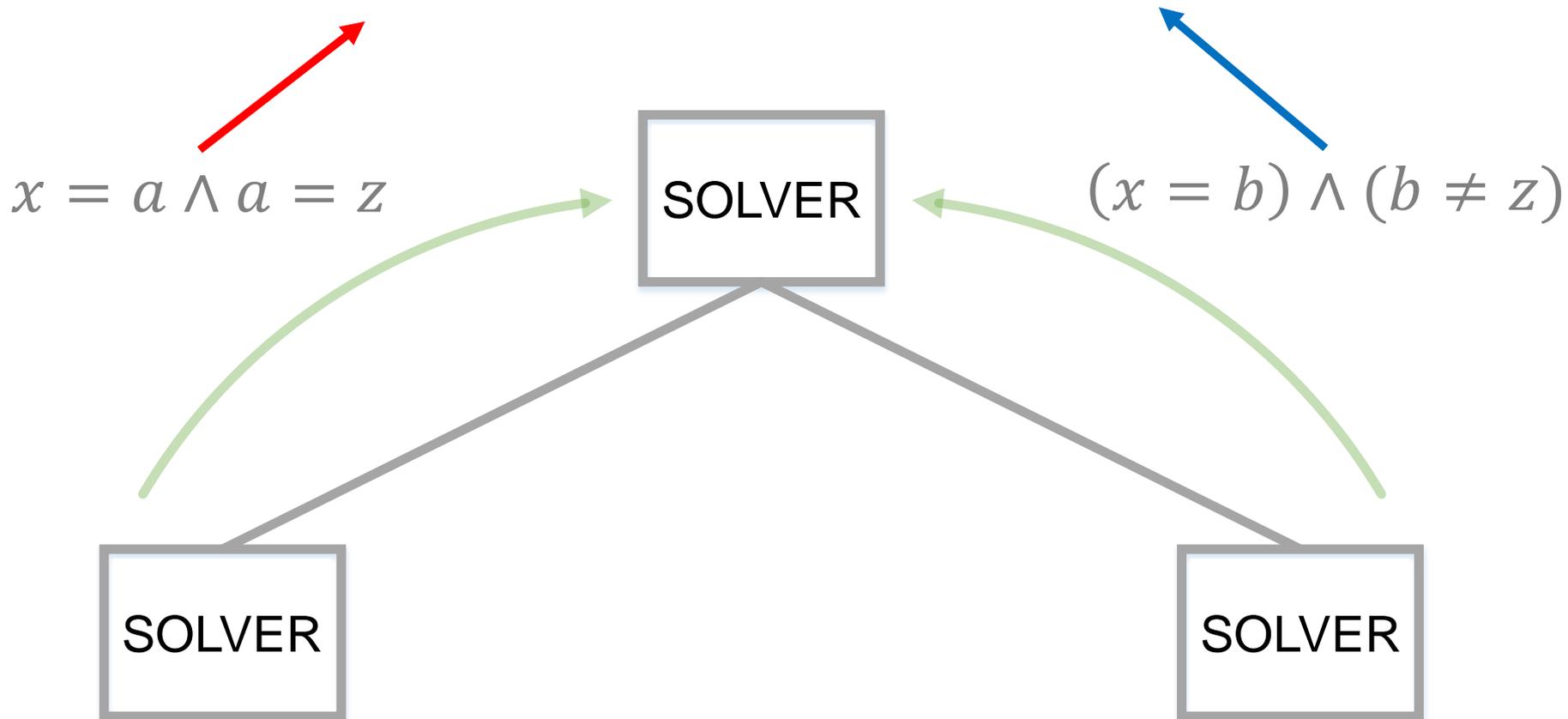


# Theory Check



# Theory Check

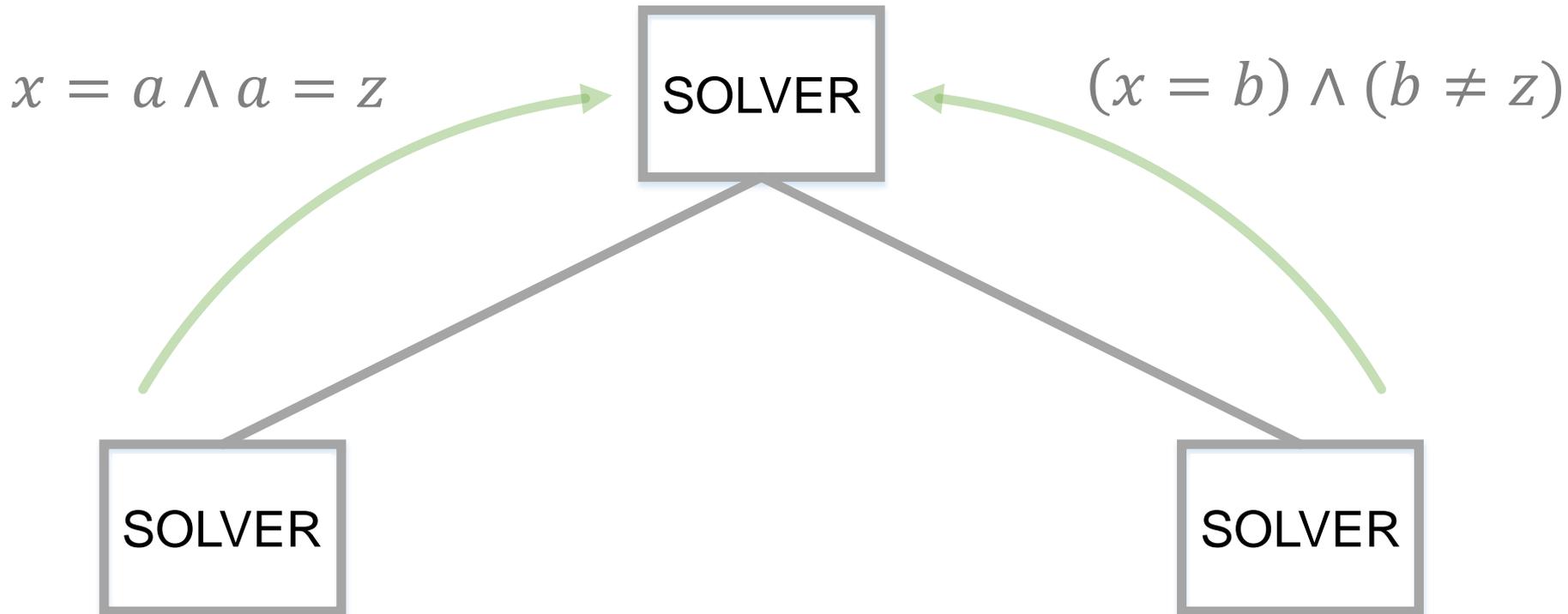
$$(x = a) \wedge (a = z) \quad \wedge \quad (x = b) \wedge (b \neq z)$$



# Theory Check

$$(x = a) \wedge (a = z) \quad \wedge \quad (x = b) \wedge (b \neq z)$$

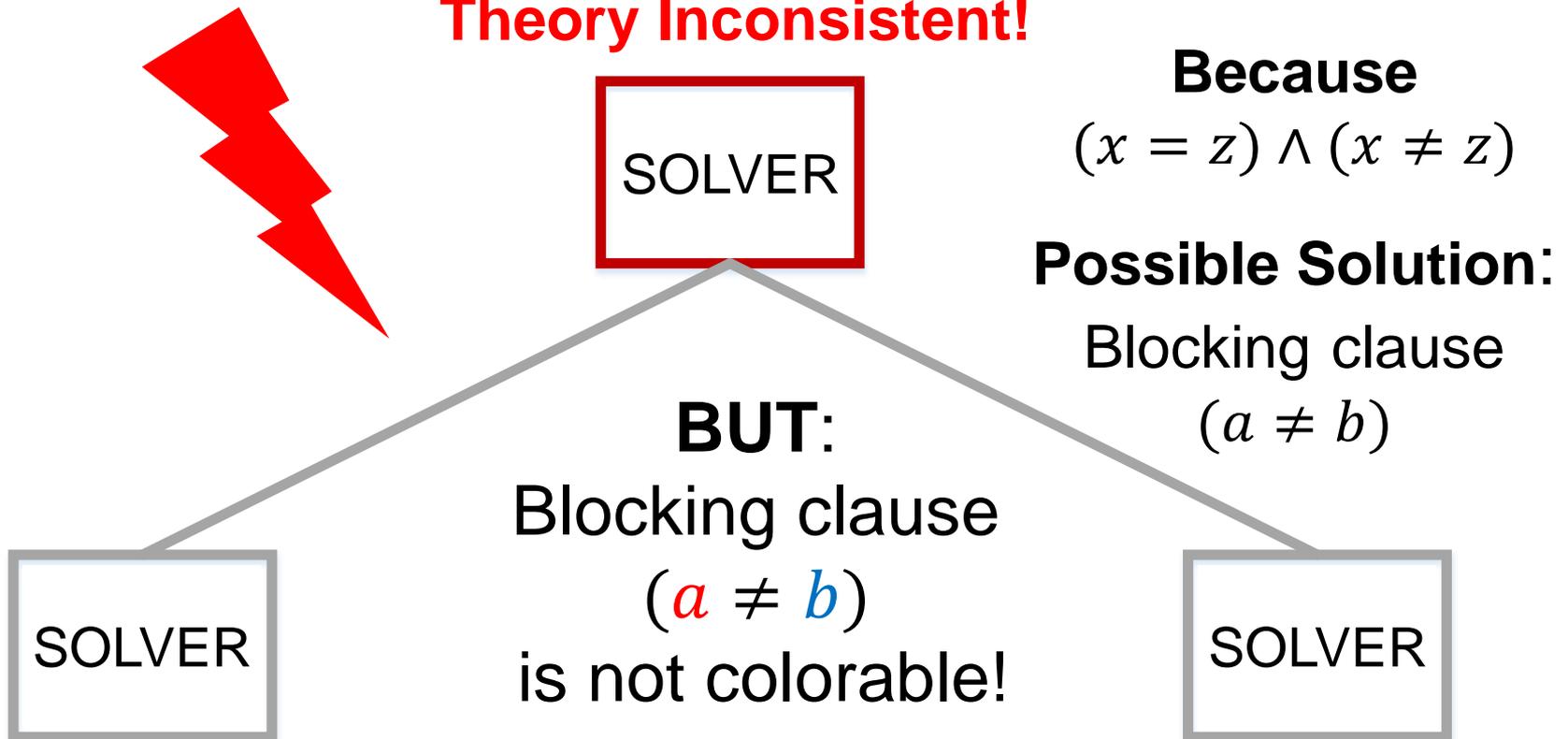
## Theory Check



# Theory Check

$$(x = a) \wedge (a = z) \quad \wedge \quad (x = b) \wedge (b \neq z)$$

**Theory Inconsistent!**



# Craig Interpolation

$$CNF(\Phi) = C_1 \wedge C_2 \wedge C_3 \wedge \cdots \wedge C_{n-1} \wedge C_n = \perp$$

A B

## Interpolant $I$ :

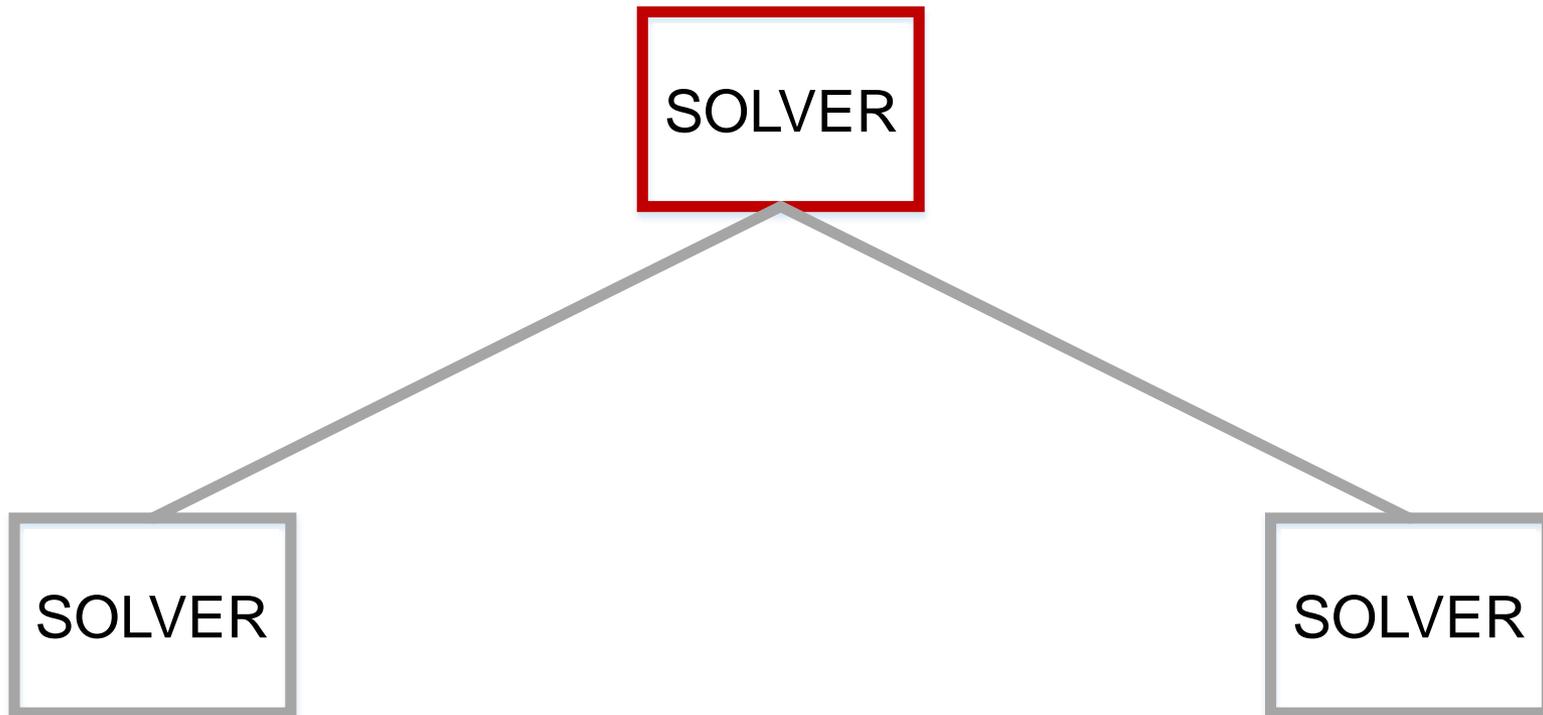
- $A \rightarrow I$
- $I \rightarrow \neg B$ , in other words:  $I \wedge B = \perp$
- $V(I) \subseteq V(A) \cap V(B)$

**Interpolant contains only global symbols.**

# Interpolation

$$(x = a) \wedge (a = z) \quad \wedge \quad (x = b) \wedge (b \neq z)$$

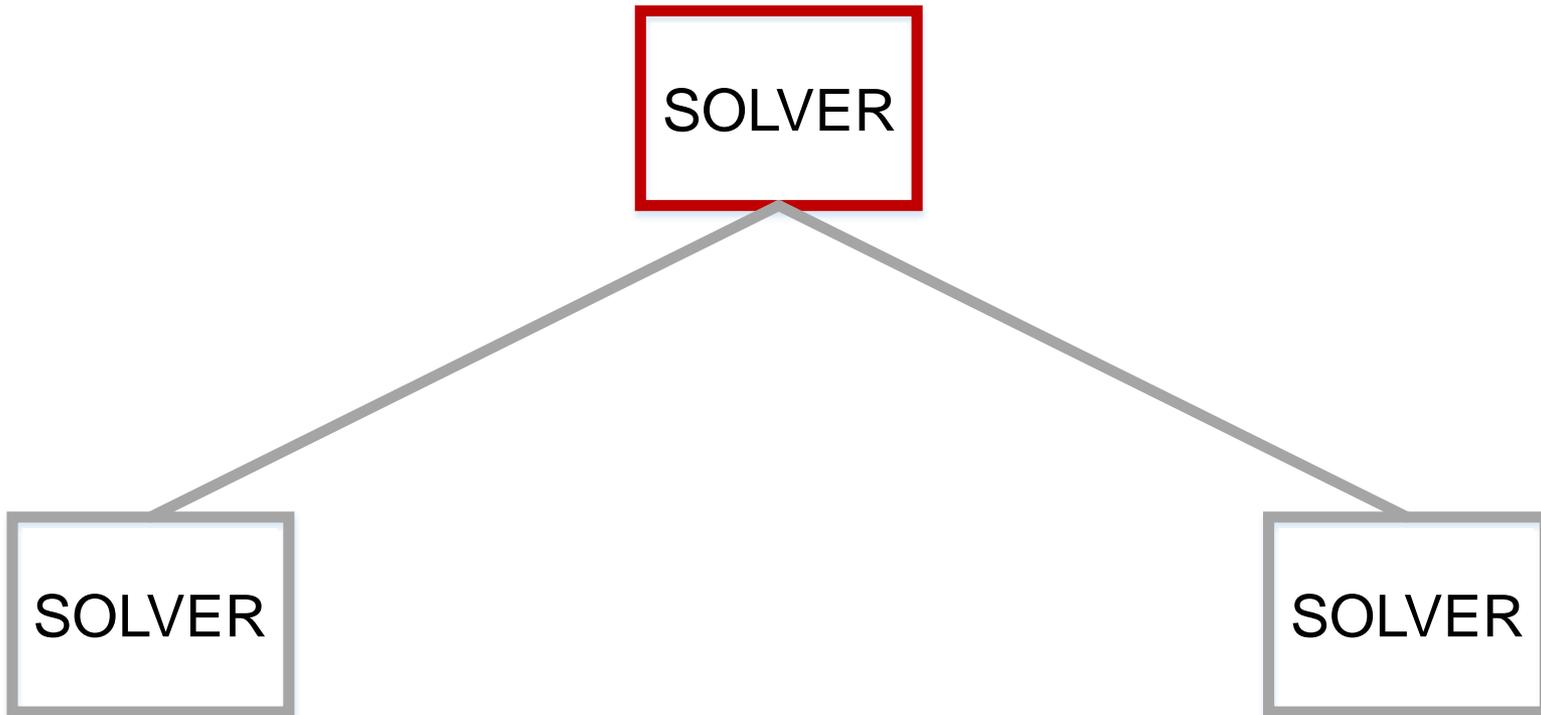
Interpolate



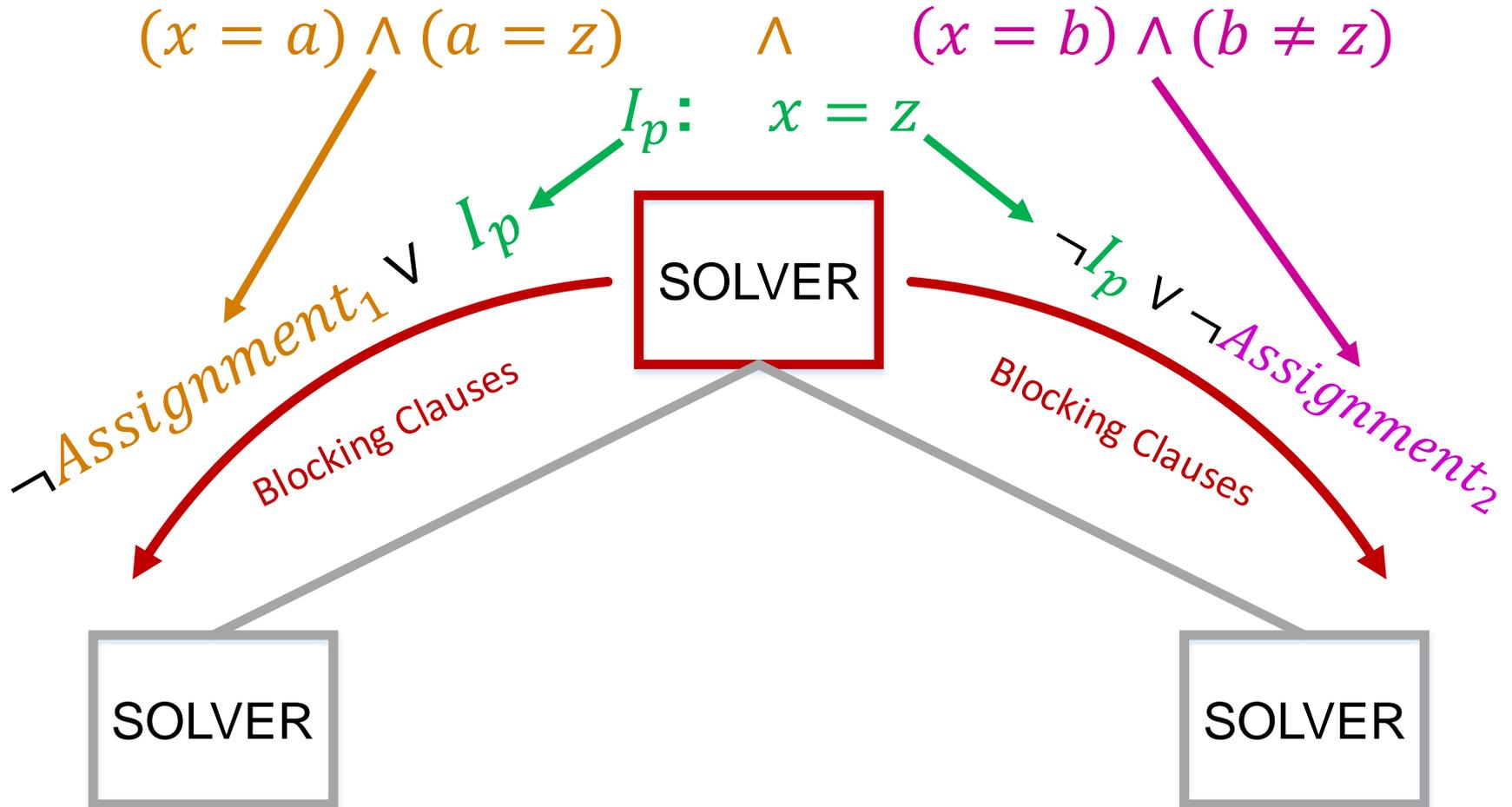
# Interpolation

$$(x = a) \wedge (a = z) \quad \wedge \quad (x = b) \wedge (b \neq z)$$

Interpolant  $I_p$ :  $x = z$



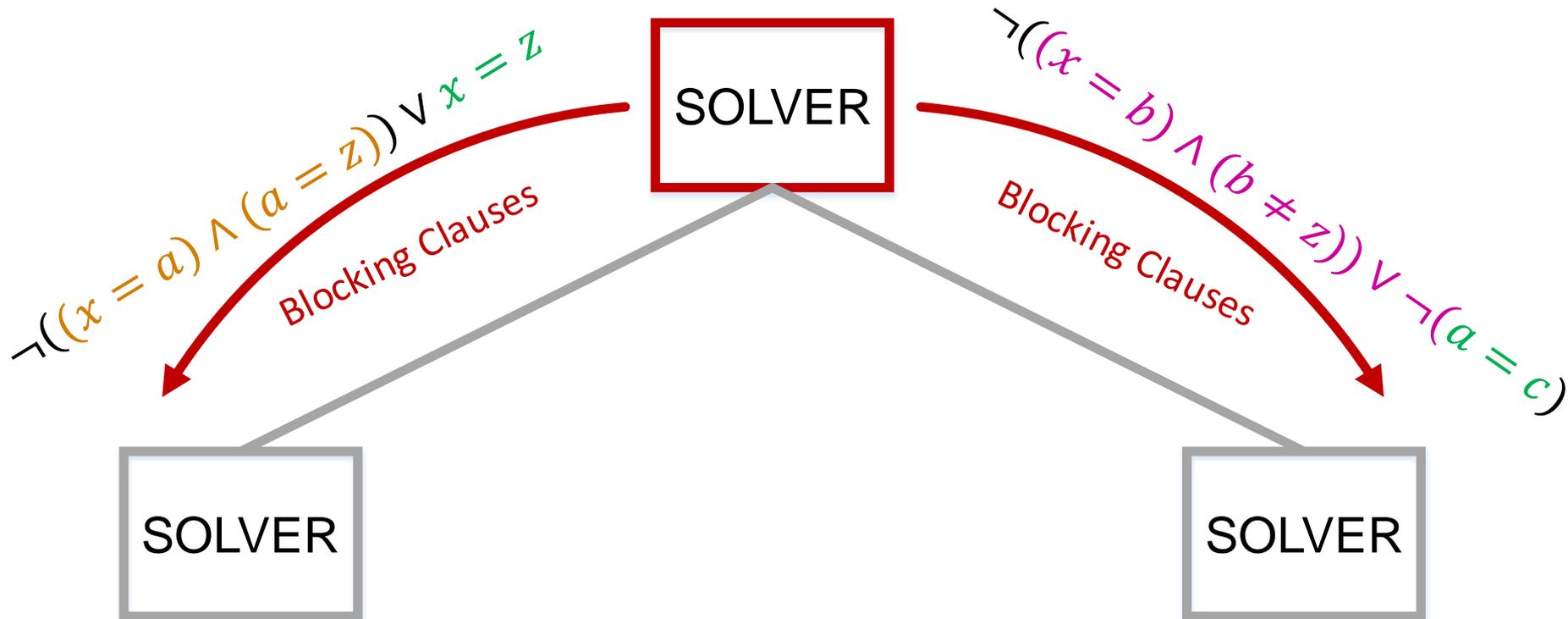
# Interpolation



# Interpolation

$$(x = a) \wedge (a = z) \quad \wedge \quad (x = b) \wedge (b \neq z)$$

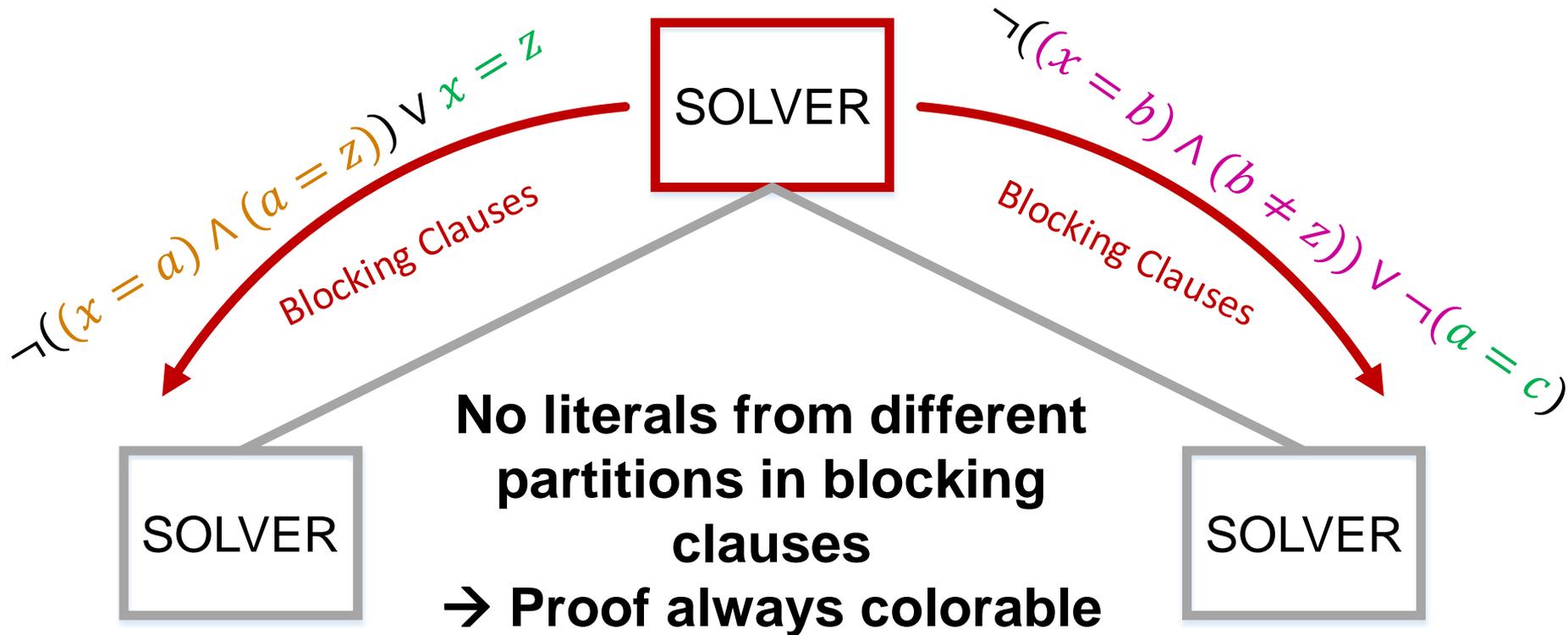
$$I_p: x = z$$



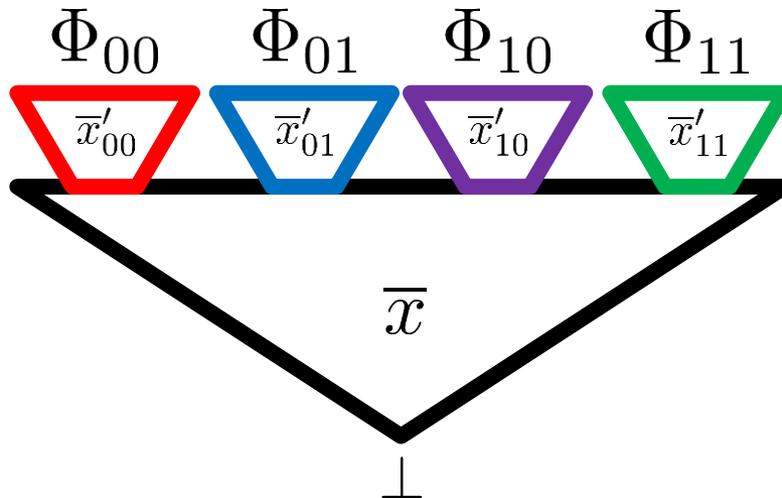
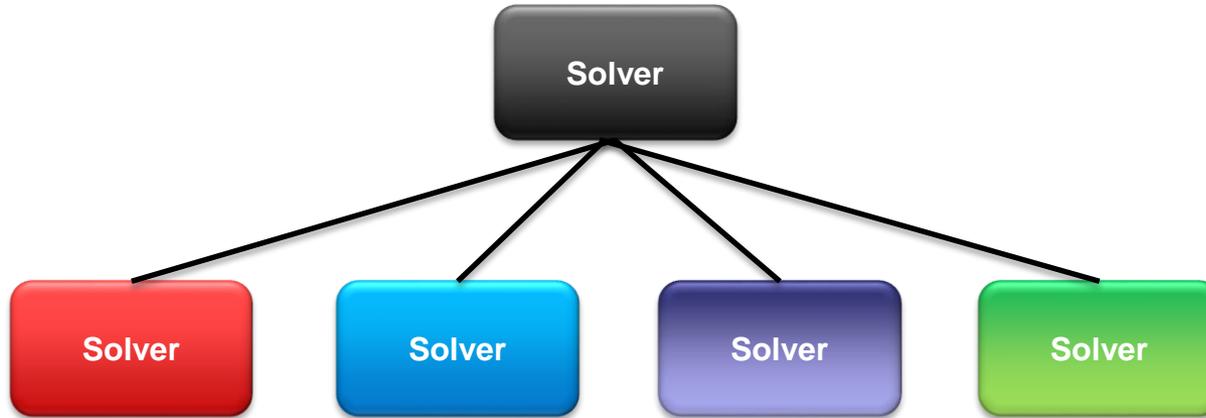
# Interpolation

$$(x = a) \wedge (a = z) \quad \wedge \quad (x = b) \wedge (b \neq z)$$

$$I_p: x = z$$



# Proof production



Root node resolves only over global literals

Premises of proof in root node are proofs of child nodes

# Current State & Outlook

- Prototype implemented („Proof of concept“) with MiniSat + MathSAT
- Relatively good runtime but much optimisation potential...
- Currently implementing proof production.

# Conclusion

- Modular SMT Solving
  - Colorable and local-first proof directly from SMT solver.
  - Possible for all theories with interpolants in same theory.
- Craig Interpolation
  - Produces colorable blocking clauses
  - Multiple coordinated interpolants from just one proof
- Therefore the world is now a slightly better place 😊

# Thank You!

Questions?



# Appendix

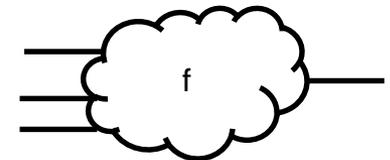
# Specification

# Specification

## Correctness: First-Order Logic Formula $\Phi$

### Important Building Blocks:

- Array Variables
  - Addressable Memories
- Uninterpreted Functions & Predicates
  - Combinational Circuits
- Domain Variables
  - Single Element Storage
  - Primary Inputs/Outputs



# Certificate via Interpolation

# Certificate via Interpolation

$$\Psi = \forall mem, reg, pipelinestate .$$

$$\exists stall, forward .$$

$$\forall mem', reg', pipelinestate' . \Phi$$

- *stall, forward*: **Boolean** control signals
- *mem, reg, pipelinestate*: Uninterpreted domain

Compute **Certificates**:

$$(stall, forward) = f(mem, reg, pipelinestate)$$

# Certificate via Interpolation

- $\Psi = \forall \vec{a}. \exists \vec{c}. \forall \vec{b}. \Phi(\vec{a}, \vec{b}, \vec{c})$ 
  - $\Psi$  is **valid**
- Function  $\vec{c} = \sigma(\vec{a})$
- Such that:  $\Phi(\vec{a}, \vec{b}, \sigma(\vec{a}))$  is **valid**

# Certificate via Interpolation

$$\underbrace{\neg\Phi(\vec{a}, 0, \vec{b}_0)}_A \wedge \underbrace{\neg\Phi(\vec{a}, 1, \vec{b}_1)}_B = \perp$$

*0 not allowed*                      *1 not allowed*

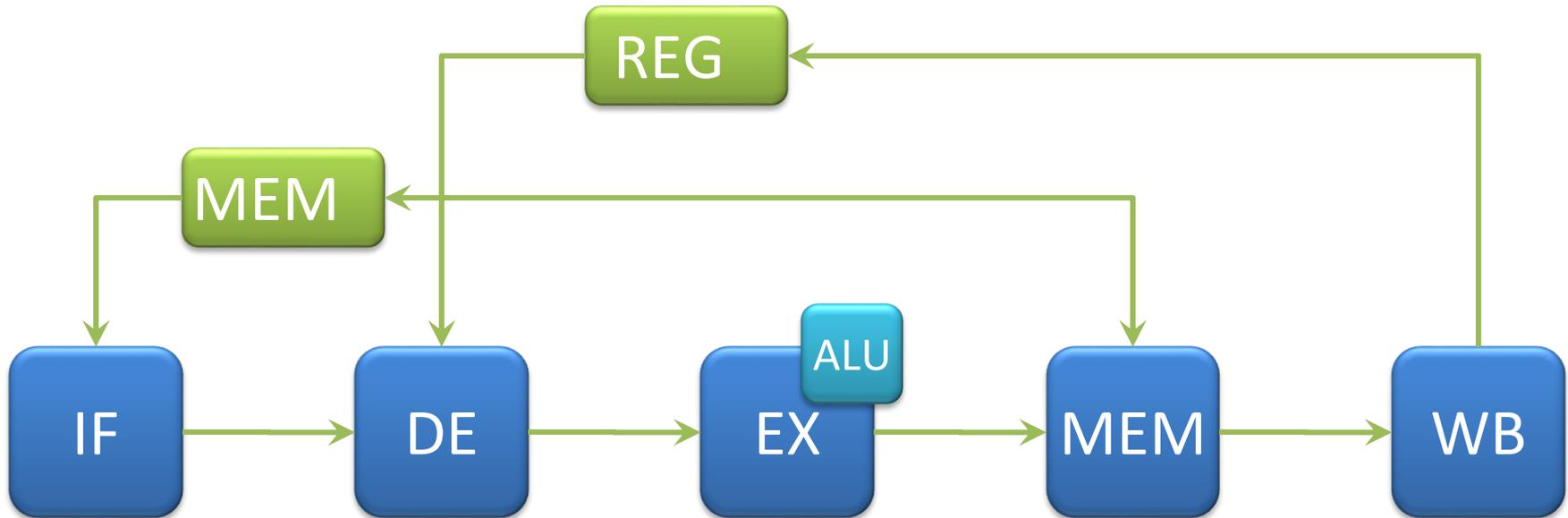
## Interpolant $I(\vec{a})$ :

- $\neg\Phi(\vec{a}, 0, \vec{b}_0) \rightarrow I$ 
  - $I$  is 1, whenever **0 not allowed**
- $I \rightarrow \Phi(\vec{a}, 1, \vec{b}_1)$ 
  - Whenever  $I$  is 1, **1 is allowed**

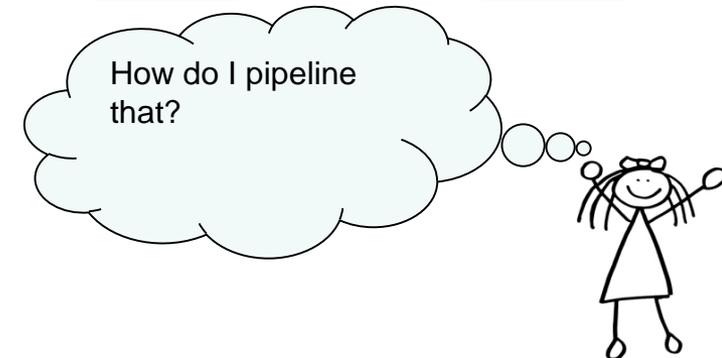
Boolean Case:  
see Jiang et al.,  
ICCAD'09

# Sample Application

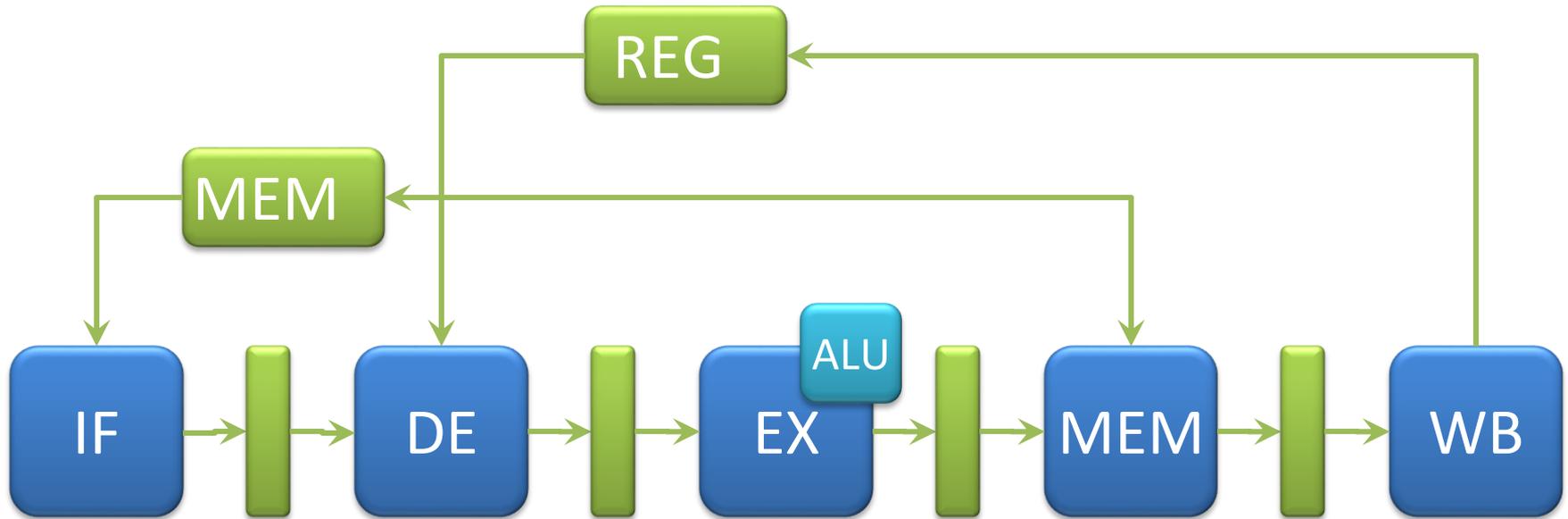
# A Processor



Tough:  
64-bit datapath  
very complex arithmetic logic unit



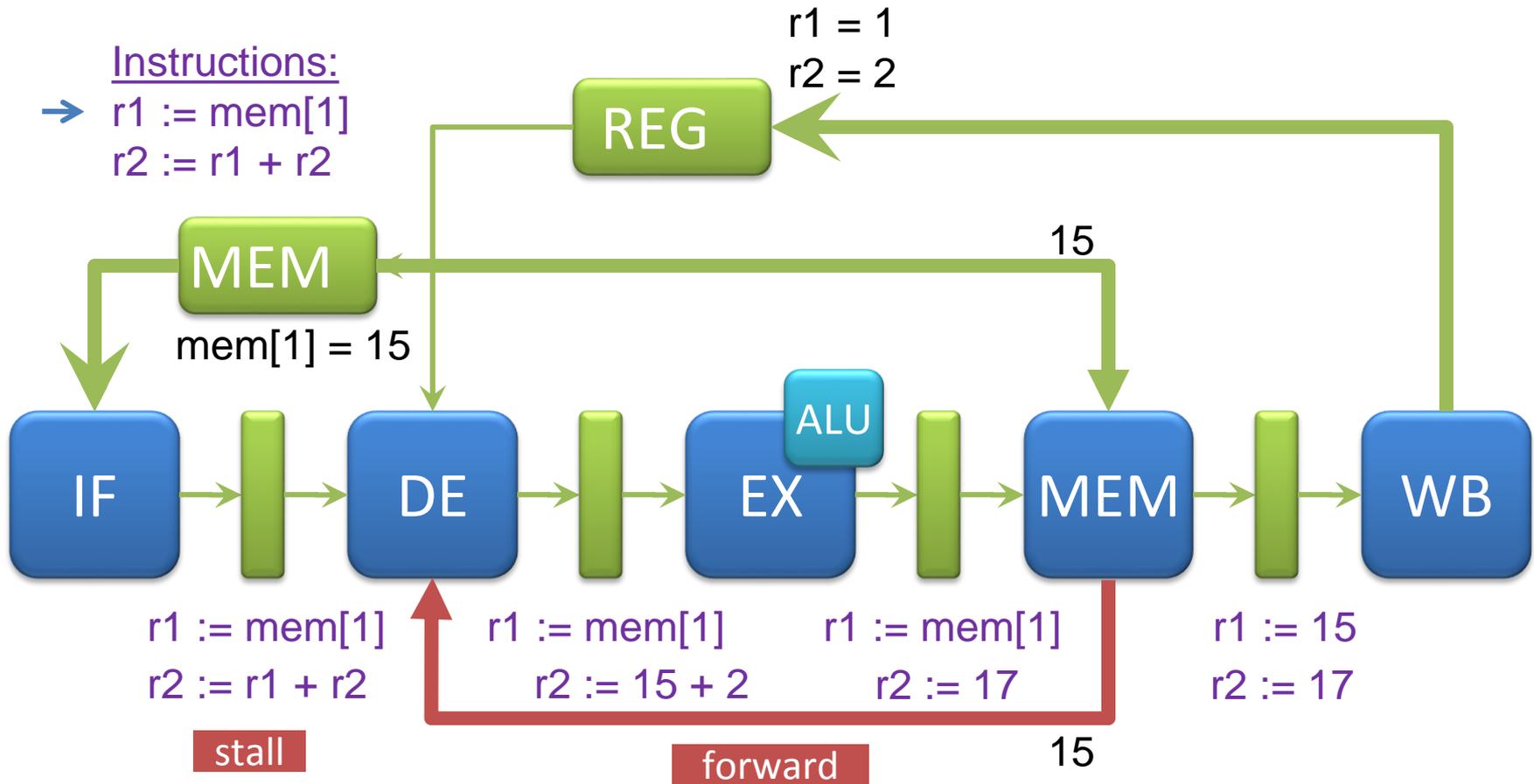
# A Pipelined Processor



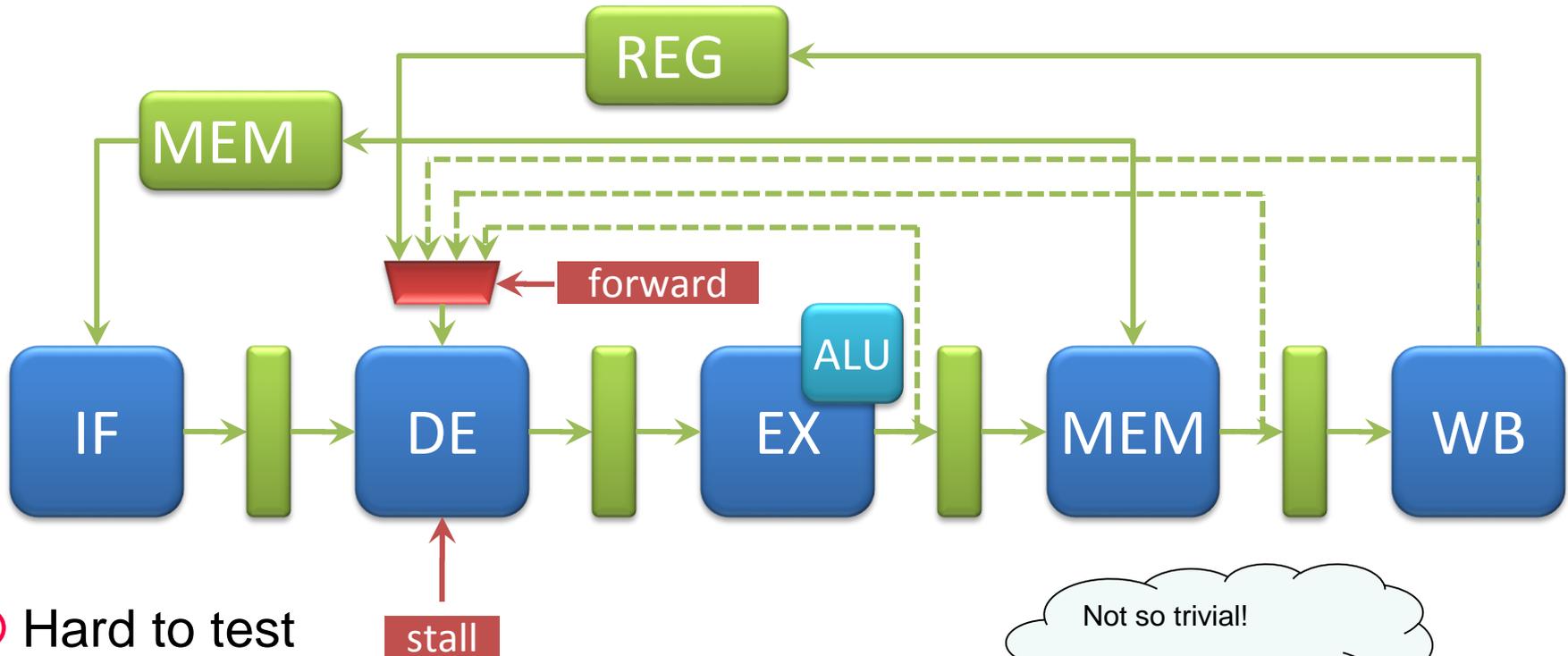
That's trivial!



# A Pipelined Processor



# A Pipelined Processor



- ☹ Hard to test
- ☹ Hard to implement
- ☺ Easy to specify → Burch-Dill paradigm



# Craig Interpolation

# Craig Interpolation

$$\text{CNF}(\Phi) = \underbrace{C_1 \wedge C_2 \wedge C_3 \wedge \dots \wedge C_{n-1}}_A \wedge \underbrace{C_n}_{B} = \perp$$

## Interpolant $I$ :

- $A \rightarrow I$
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