EasyChair Preprint

№ 10887

A Bondwire Inductor Based Flash ADC Assisted DC-DC Buck Converter

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September 11, 2023

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***Abstract*— A flash ADC-assisted fast transient response DC-DC buck converter is proposed in this paper. The proposed inductor-based DC-DC converter operates in continuous conduction mode (CCM). The novelty in architecture includes replacing SAR ADC with Flash ADC which converts the transient overshoot/undershoot into corresponding binary code at a faster rate as compared to SAR ADC. Depending on the overshoot and undershoot set criteria, the current pump injects the current into the output node to charge /discharge the output node to minimize the overshoot/undershoot and settling time. In the proposed design, required inductance is achieved by using bond-wire inductance, which reduces the chip's active area, and off-chip components. ADS simulations are performed for estimation of inductor values using the QFN-64 package. The proposed DC-DC converter occupies an active area of 0.91mm^2 using TSMC 130 nm bulk CMOS process. Post layout simulation results show the peak efficiency of 84% at V_{in} of 3.3 V, V_{out} of 1.8 V with the load current I_L of 500 mA. The measured overshoot/undershoot in simulation is 70/60 mV with 530/469 ns recovery time and 7 mV output ripple. This enables the designed converter to be used in applications like aerospace, satellite, as well as military applications, where compactness is required.**

***Keywords*— DC-DC Power Converters, Flash ADC, Current pump, Buck converter, Continuous Conduction Mode, Bond-Wire based Inductor, IoT Applications.**

I. Introduction

Electronic circuits are energized by batteries, which provide fixed voltage. However, various sub-components of an electronic system operate efficiently at different voltages, other than battery voltage. Thus, for efficient operation, rather than directly biasing from the battery, circuits are biased at optimal operating voltage by DC-DC converters [1]. Highly stable power supplies are widely used in communication, the Internet of Things (IoT), medical equipment, aerospace, and defense systems as shown in Fig. 1.

On-chip DC-DC converter provides a compact, efficient, precisely controlled, and fast transient response biasing supply, so is quite feasible for such an application [2]. The elimination of large off-chip components i.e., power switches, off-chip inductor, etc. not only helps to reduce the area but also make it a cost-effective solution. Besides the power efficiency, the circuits operating over a wide frequency range, experience current variation under different loading conditions i.e., heavy and light. The dynamic behavior causes the current of the system to change abruptly, leading to the phenomenon of voltage overshoot or undershoot, which degrades the overall system's performance [3]. As the technology node is shrinking, low voltage operation is being adapted i.e., 65nm Bulk CMOS works typically at 1.2V. So, due to low voltage operation along with increasing switching frequency, it becomes more challenging

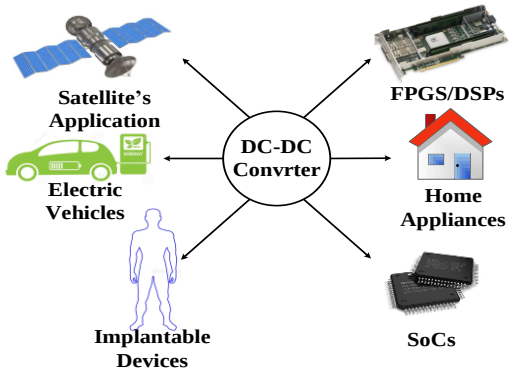

Fig. 1. Applications of DC-DC converters

to design an on-chip DC-DC converter to achieve a fast-transient response [4], [5]. Therefore, in addition to efficiency, overshoot/undershoot, settling time, and output voltage ripple are essential quality parameters of DC-DC converters.

Different state-of-the-art designs have been presented over the past years to improve the transient response of the inductor-based DC-DC converters. The work reported in [6] presents a four-phase DC-DC converter scheme to address both issues. Although the output ripples are greatly decreased, it requires an accurate current sensor and a current balancing circuit are necessary for the multiphase pulse-width modulation (PWM) control. The solution presented by [7] overcomes the above problems with a time-based PID control (T-PID) in the multiphase design. However, the performance of T-PID control has a close relationship with voltage control oscillators (VCOs), which suffer from process and temperature variations. To further increase the load transient performance, [8], [9] proposed a load transient optimizer in the control loop of the multiphase buck converter that senses the output capacitor current. A different approach for this purpose is utilized in [10], where a programmable current pump, digitally controlled by a 4-bit SAR ADC optimizes the transient response and recovery time. However, SAR ADC requires multiple clock cycles for digital output generation, which limits transient response and recovery time.

II. Proposed System Architecture

This section describes the proposed fast transient response DC-DC converter. Transient performance is improved by replacing SAR ADC with flash ADC, which converts the analog signal into a digital signal using single cycle, while considering the tradeoff with respect to area, power and speed. Detailed operation of the sub-blocks of proposed solution, i.e., op-amp, comparator, current pump and windowed flash ADC is elaborated in the preceding sub-sections.

High load current favors continuous current mode (CCM), which eliminates the requirement of the zero-cross detection (ZCD) circuit. A type-III compensator is opted to ensure less than 10 mV output ripple. It not only reduces the output voltage ripples but also increases the system's stability, as well as removes the requirement of programmable current pump compensator, as given in [11]. Top level architecture of the proposed DC-DC converter, which provides fast transient response by using flash ADC is shown in Fig. 2. A Folded Cascode OP-AMP shown in Fig. 3 is used to generate error signal as well as provide stability to the whole system by adding poles and zeros in to the system i.e., by creating Type III-B compensator. The error is then compared with sawtooth wave using cross couple comparator to generate the desired PWM. The schematic of cross coupled comparator is shown in Fig. 4. A windowed flash ADC converts the overshoot/undershoot into their respective digital signals, which injects in/draw out the current from the system using current pump, thus, improving the overall transient response of the system.

Description of the modules used in the proposed design is providing in the following sub-sections.

A. *Power MOSFET*

The selection of suitable size of MOSFET switches play an important role in efficiency of system's performance. The major types of losses in the power switches are conduction losses and switching losses [12]**.** Under light load condition switching loss are dominant, which is reduced by smaller switch size. Whereas, under heavy load conduction loss is dominant [13]. Hence to reduce the conduction losses, the size of the transistor should be increased at heavy load, which in turn increase the switching losses. Thus, switch sizing is done on trade-off analysis between conduction and switching loss. For a 90% efficient DC-DC converter, the on-resistance of switches can be calculated as shown in (1) and (2) [6].

$$P_{loss} = \left(\frac{P_{out}}{100}\right) * (1 - \eta) \quad (1)$$

$$R_{loss} = \frac{P_{loss}}{R_{load}{}^2} \quad (2)$$

Where η is the efficiency of the system.

B. *Folded Cascode - Common Source (FC-CS) Op-Amp in Type III-B Compensator*

The DC-DC Converter's stability hugely depends on the op-amp crossover frequency (f_c), which is usually $\frac{1}{5}$ to $\frac{1}{10}$ times the switching frequency. Transient performance improves at the higher f_c. To achieve the higher performance with good stability, the gain of the op-amp should be as high. To achieve a high slew rate, the bandwidth of op-amp should be high as well, such that the value of f_c lies inside the 3dB bandwidth of DC-DC converter. However, there is an inverse relation between gain and bandwidth, hence, a tradeoff is required between gain and bandwidth.

Fig. 3 shows the schematic view of folded cascode op-amp. The 3-dB bandwidth of folded cascode op-amp is wide with medium gain, which meets the requirements of our proposed system. The op-amp consists of two stages, biasing voltage generation and gain generation. M10 along with M11 generate bias voltage, while M12, M13, M14, M15 and M16 are used for biasing voltage generation and current mirroring. The input pairs M1 and M2 are the main transistors, determining the gain. Their trans-conductance (g_m) has a

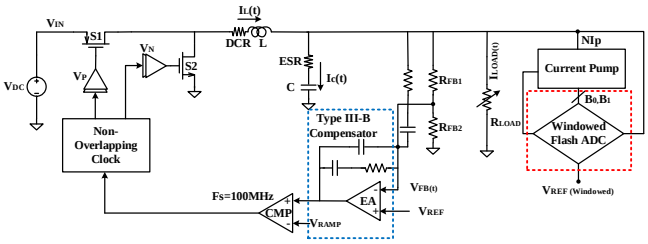

Fig. 2. Top-level architecture of the proposed fast transient response DC-DC converter using flash ADC

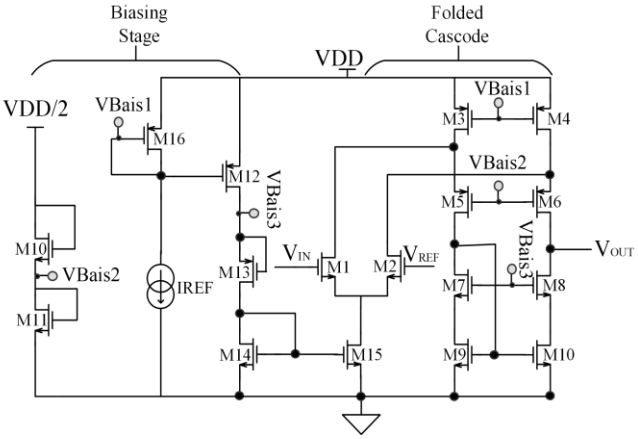

Fig. 3. Schematic of folded cascode op-amp

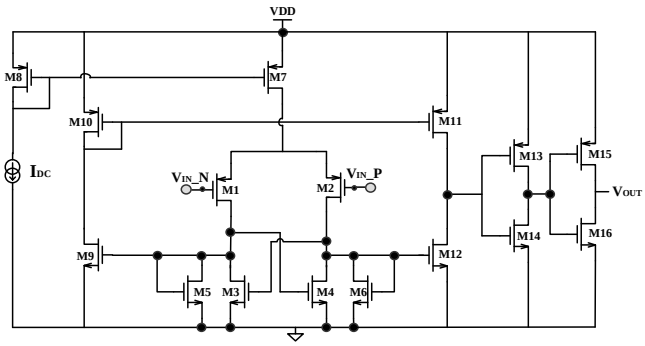

Fig. 4. Schematic of cross-coupled loaded comparator

direct effect on the overall gain of the op-amp. M3, M4, M5, M6, M7, M8, M9 and M10 determine the output resistance of the op-amp. The expression for the op-amp gain (A_{v_AMP}) is given in (3), where r_o is the output impedance of the transistor, and g_{mb} represents the body transconductance of the transistor. Expression (3) shows, in addition to g_m, A_{v_AMP} can be increased by increasing output transistors r_o.

$$A_{v\_AMP} = g_{m1}\{[(g_{m5} + g_{mb5})r_{o5}(r_{o1}||r_{o3})]||[(g_{m7} + g_{mb9})\, r_{o7}r_{o9}]\} \quad (3)$$

The objective of compensator design is to compensate the closed-loop system such that the phase at 0 dB gain is greater than 45°-60°. There are usually three types of compensators in the literature i.e., Type I, Type II and Type III-A/B [14]. Type I compensator is not used in high frequency application because of its fixed poles zeros presence at fc. The selection of Compensator depends upon the presence of the poles and

TABLE I. TYPES OF COMPENSATORS [14]

Compensator Type	Relative location of poles
Type II (PI)	$F_{LC} < F_{ESR} < F_o < F_{s/2}$
Type III-A (PID)	$F_{LC} < F_o < F_{ESR} < F_{s/2}$
Type III-B (PID)	$F_{LC} < F_o < F_{s/2} < F_{ESR}$

zeros due to the presence of ESR of output capacitor, which can be depicted from the Table I.

Here F_{LC} is the resonance frequency of the power stage of the Converter, F_{ESR} is the pole frequency due to ESR of the capacitor, F_o is the centre frequency of the Converter and F_s is the switching frequency of the Converter.

C. High Speed Comparator

A cross coupled comparator is designed for producing the desired PWM signal. The schematic of the cross-coupled comparator is shown in Fig. 4. Comparator uses internal positive feedback to increase the gain, followed by a differential to single-ended conversion along with two inverters to improve the driving capability of the circuit and provide rail to rail swing. M8 and M7 mirror the source current. M1 and M2 act as a source coupled differential input pair. M3, M4, M5 and M6 function as the cross-coupled bi-stable load for the differential input stage. The current difference produced in M3, M4 is converted into voltage with the help of transistors M9 and M12. The current of transistor M9 is then mirrored to M12 with the help of M10 and M11 transistor. Which after passing through buffer converts a differential input to a single-ended output having high output driving capability. The size of current mirrors that transform the differential output to single-ended can be made small to reduce the parasitic capacitances at their gates for a faster response. The mathematical expression for gain (A_{v_CMP}) of the first stage is given in (4).

$$A_{v\_CMP} = \sqrt{\frac{\mu_n (W/L)_{M2}}{\mu_p (W/L)_{M4}}} \cdot \frac{1}{1-\alpha} \quad (4)$$

Here, α is a constant known as the positive feedback factor responsible for increasing the gain. A reasonable value for α is around 0.75, which increases the gain by a factor of 4, and is determined by the ratio of the load transistor (M3, M4) dimensions. It is desired that this value stays below one, as at α =1, the comparator converts to a latch, and for values α >1, it behaves as a hysteresis comparator. The mathematical expression for the value of α is given in (5).

$$\alpha = \sqrt{\frac{(W/L)_{M3}}{(W/L)_{M4}}} \quad (5)$$

The main parameters in any comparator are propagation delay and offset error. The propagation delay and offset error is 170 ps and 20 mV, respectively.

D. Current pump

The designed current pump is shown in Fig. 5 (a), which pull-up or pull-down the V_{OUT} by switch controlled current sources. The overshoot and undershoot threshold are predefined in the ADC, that generate the 2-bit digital signal, which controls the switching activity, i.e., when undershoot occurs, let suppose 50mA current is withdrawn through the circuit to mitigate undershoot as well as the settling time and vice versa. As long as the output remains within the threshold limits, the current pump will not provide current to the system. During overshoot V_{OUT} (flash ADC V_{in}) exceeds V_{ref+} which turns on pull down path of the current pump, until V_{OUT} pull-downs to the pre-defined hysteresis window. Similarly, during undershoot pull-up path is triggered for mitigation.

The mitigation of overshoot and undershoot depends upon the turn-on time T_{on} of the current pump. If T_{on} be the time

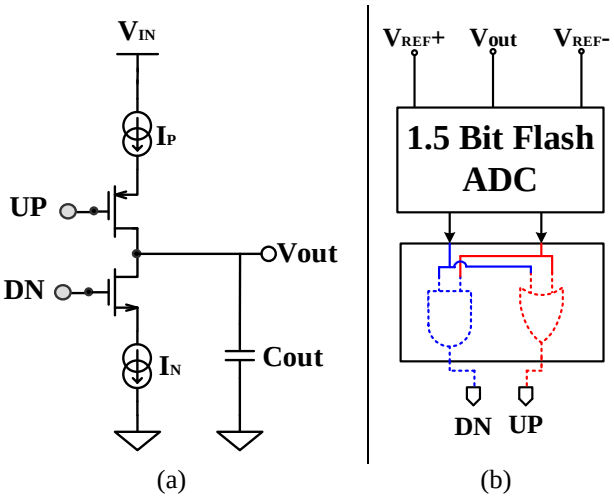

Fig. 5. (a) Fixed current pump architecture for proposed design (b) Windowed flash ADC in the proposed architecture

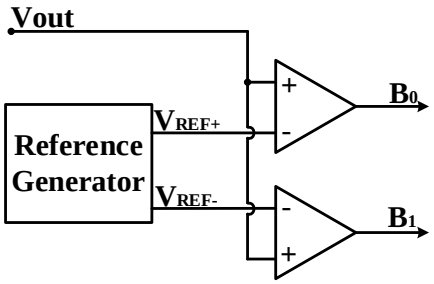

Fig. 6. Proposed architecture of windowed flash ADC

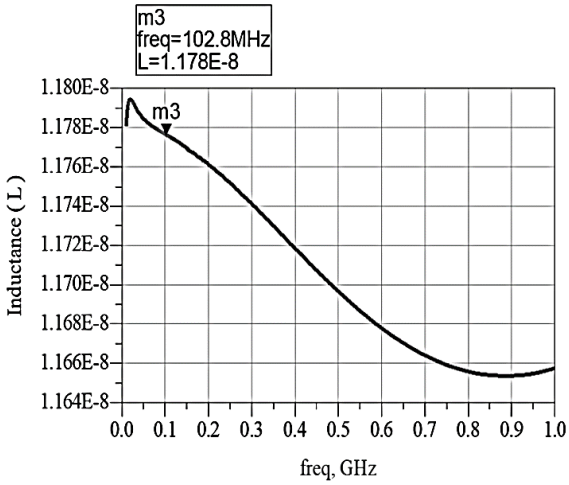

Fig. 7. ADS simulation showing bond wire inductance at 100MHz

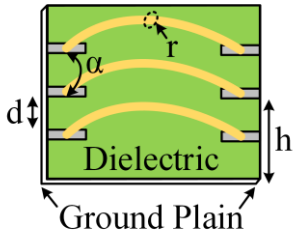

Fig. 8. The concept of Inductor Modelling using bond-wire from die pin to package pin.

for which the current pump turns on and Q is the charge transferred during this T_{on} period, then the overshoot or undershoot mitigation voltage (V_{cp}) is given in (6).

$$V_{cp} = \frac{Q}{Cout} = \frac{I_p.T_{on}}{C_{out}} \quad (6)$$

Here, I_p is the average current transferred during T_{on} and C_{out} is the output capacitance of the DC-DC Converter.

E. Windowed Flash ADC

As shown in Fig. 2, an ADC is required to convert analog output voltage into digital binary bits, which controls the charge pump's current. There are many analog-to-digital converters based on different design methodologies. Among these different techniques are Sigma Delta ADC, SAR ADC, and flash ADC [15]. Flash ADC employs parallel architecture, which consist of comparators and binary encoder, and is the fastest ADC. Comparators generate thermometer code, while a binary encoder is used to convert the thermometer code. The major drawback of the flash ADC is high area because of the N comparators. A 1.5bit flash ADC is employed in this design to meet the desired target as at it occupies only a small fraction of the total active area of the proposed architecture. The 1.5-bit flash ADC uses two comparators and a set of AND and OR gate to turn on and off the current pump. Windowed Flash ADC is used to limit the operation within specified voltage range (overshoot/undershoot). Multiple architectures of windowed flash ADC are proposed in current literature [16]–[18]. In order to meet the speed requirements as well as PVT variations, the proposed ADC uses two rail to rail comparators along with references generator to operate within the specified voltage range.

It operates in three regions i.e., overshoot region (11), undershoot region (00) and in bistable region (01, 10). During the overshoot and undershoot, the windowed flash ADC would turn on the current pump and current will inject in/draw out. While in the bistable state, the current pump remains off and no action takes place. Fig. 5 (b) and Fig. 6 shows the block level and schematic of windowed flash ADC, where V_{ref+} and V_{ref-} are selected based on the overshoot and undershoot requirements of the design.

F. Inductor Modeling

The inductor (L) is an integral part of the DC-DC converter as the filter stage of the DC-DC converter consist of an inductor and a capacitor. The major concern for on-chip DC-DC converter is the large on-chip inductor area, which might take up to 50-60% of the active area. A 30 MHz operating inductor-based DC-DC converter requires 240 nH on-chip inductor, occupying an area of 4 mm^2, with a quality factor of 4. This area is too large, which increases the product cost. A bond wire can be used to achieve the desired inductance [19]. [11], [20]–[23] used this approach to implement the inductance of the filter with bond wire, which is opted in this design. ADS simulations are performed on the QFN-64 package to obtain the desired results. Bond wires are connected in series to achieve the desired inductance of ≈10 nH. Zigzag arrangement of the bond wires causes mutual inductance as well, which increases inductance.

The stack is built with different values of dielectric material to model the FR4 PCB over which the QFN-64 package is modelled. The mathematical expression for self-inductance of a bond wire is given in (80 while the expression for mutual inductance of straight wire pair is given in (9), where μ_o is the permeability in a vacuum (4π x 10^{-7} H/m), h is the height above the substrate, r is the wire radius, d is the distances between wires and μ_r is the relative permeability (dimensionless) [24]. Fig. 7 shows the ADS simulation. Which shows 12 nH inductance at 100MHz. A 20% margin has been provided so that in the worst-case scenario, the achieved inductance should be 10 nH or greater than 10 nH to ensure the CCM of the converter. Fig. 8 gives a view of inductor modelling using bond-wire.

$$L = \frac{l\mu_r\mu_o}{2\pi}\ln\left(\frac{2h}{r}\right) \quad (8)$$

$$L_m = \frac{l\mu_r\mu_o}{4\pi}\ln(1+[\frac{2h}{d}]^2) \quad (9)$$

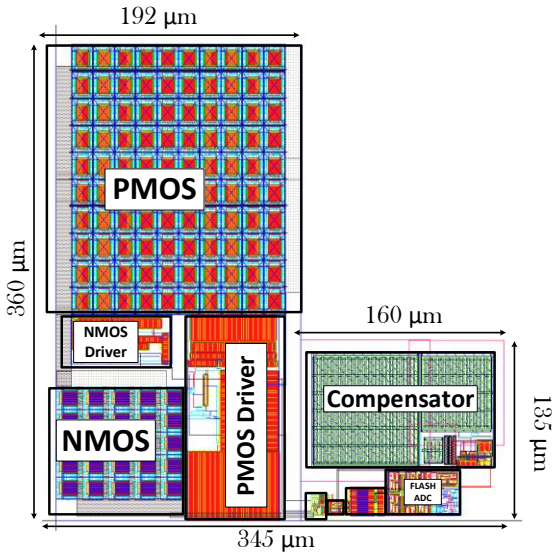

Fig. 9. Layout of proposed flash ADC based current pump assisted DC-DC converter

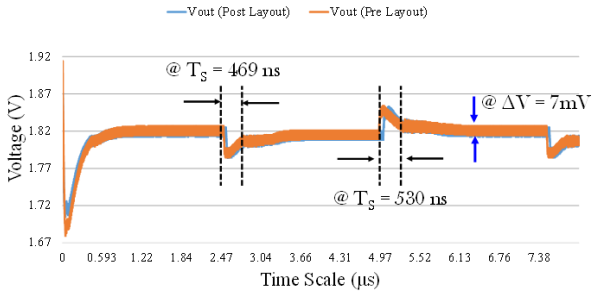

Fig. 10. Waveform of DC-DC converter when load is varied from 20mA to 400mA and vice versa

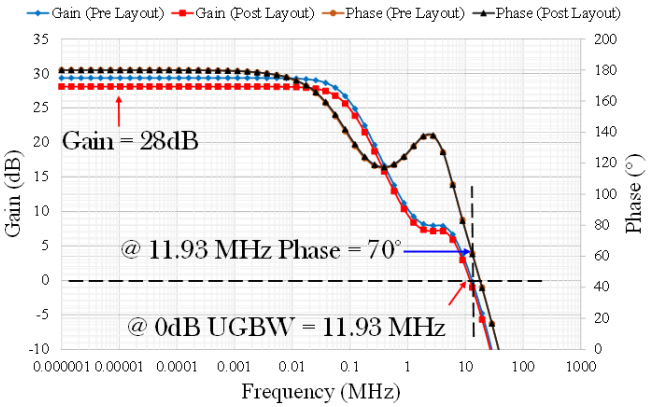

Fig. 11. Small signal analysis of flash ADC based current pump assisted DC-DC converter

III. Simulation Results And Comparison With State- Of-the-Art DC-DC Converters

The proposed design initially simulated in the MATLAB Simulink, and then the transistor level architecture is designed and simulated in Cadence Virtuoso using 130nm Bulk CMOS technology. The top-level layout of the proposed DC-DC converter is shown in Fig. 9. The proposed DC-DC converter occupies the active area of $0.91mm^2$.

The major problem associated with this proposed converter is the substrate switching noise, making the overall system unreliable. Therefore, in order to reduce the substrate noise, each module has its own guard ring, especially the power transistors. Similarly, the routing over the critical modules is made as less as possible. If it is necessarily required, then the routing is done on top metal layers.

Load variation post layout simulation results are presented in Fig. 10. It can be observed; the transient performance of the system has been improved. The overshoot/undershoot of proposed design is 70/60mV with 530/469ns recovery time, and 7 mV ripple voltage. Likewise, Fig. 11 shows the stability analysis of proposed DC-DC converter architecture. The f_c of proposed design is 11.93 MHz with phase margin of 70°. Which indicates that the proposed designed is highly stable. A well-compensated DC-DC converter is crucial for any practical use. Hence, small-signal analysis needs to be performed on proposed converter's loop. However, it is difficult to do the loop analysis as the PWM is varying signal, and it operates in the large signal mode. Thanks to STB, PSS, PSTB, PAC simulations given in the Cadence ADEL environment because by using these tools small signal analysis can be realized.

Table II shows comparison of proposed design with state-of-the-art fast transient DC-DC converters. The results show a significant improvement in the performance of proposed DC-DC converter with other state of the art designs. The proposed DC-DC converter achieves peak efficiency value of 84% at $I_L = 500mA$, when Vin = 3.3V and Vout =1.8V. The simulated overshoot/undershoot value for the proposed converter is 70/60mV with 530ns/469ns recovery time.

TABLE II. Comparison of proposed design with state-of-the-art fast transient DC-DC converters

	This Work	[23] **2013**	[11] **2020**	[20] **2018**	[19] **2015**
Process	130nm	130nm	65nm	180nm	65nm
Control	PWM	PWM	PWM	PWM	T-PID PWM
Input Voltage (V)	3.3	1.2	1.2V	1-2.7V	1.8V
Output Voltage (V)	1.8	0.6-1.05	0.6-1	3.2	0.6-1.5
Switching Frequency (MHz)	100	100	100	118	30-70
Inductance (nH)	10	11	10	20	90
Capacitance (nF)	100	7.5	15	1.08	470
Load Current (mA)	300	1200	100	65	800
Load Transient Step (mA)	20-400	20-200	2-50	6-40	100-500
Overshoot/ Undershoot (mV)	70/60	60/40	101/92	192/130	80/80
Peak Efficiency	84%	82.4%	81%	77.4%	87%
Settling Time (ns)	530 /469	800 /1000	175 /310	650 /650	600 /600
Area (mm^2)	0.91 (without PADs)	1	1	0.52	1
FoM = $\frac{\text{Settling Time (ns)}}{\text{Load Step (mA)}}$	1.1 /0.98	4.44 /5.56	3.64 /6.46	19.12 /19.12	1.5 /1.5

IV. Conclusion

In this work a PWM controlled inductor-based DC-DC converter, operating in CCM mode, using bond-wire inductance, and flash ADC is presented, which achieves fast-transient response during the load transient. As the implemented flash ADC performs conversion in single cycle, the conversion speed is very high as compared to other types of ADC. A total inductance of 10nH with 20% margin is achieved using bond wire, which is verified through ADS simulations. During the load transient, a 1.5-bit flash ADC controls the current pump. Depending upon the values of overshoot/undershoot, it enables the current pump to charge and discharge the output node. Digital code b_0b_1 = 11 represents overshoot, while b_0b_1 = 00 represents undershoot. The proposed converter design achieves peak efficiency of 84% at I_L(500 mA), when Vin is 3.3V and Vout is 1.8V. The simulated overshoot and undershoot values are 70mV and 60mV respectively, with recovery time of 530ns/469ns.

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